Errata: CS4207 Rev. C0/C1/C2 Silicon

(Reference CS4207 DS880F4 Data Sheet)

1. BEHAVIORAL PROBLEMS

1. Presence detect changes during link shutdown do not always generate an unsolicited response when the link is resumed. When the link is shut down (controller in D3, RESET# low, BITCLK off) and a change in the Presence Detect (PDET) status occurs, the codec correctly issues a power-state change request (SDI high); however, it fails to generate an unsolicited response if an even number of Presence Detect changes occurred, i.e., if the actual Presence Detect state is the same at wakeup as it was before shutdown. Since no unsolicited response was issued, the UR event remains pending internally and causes another power state change request as soon as the link is shut down again. This scenario repeats until the pending UR event is cleared. The problem here is not that the host would miss a Presence Detect state change (since the net change is actually 0 in this case), but rather that the never-ending assertion of power-state change requests (wake events) by the codec.

   If an odd number of presence detect changes occurred during link shutdown, the proper unsolicited response is generated and the pending UR event is cleared.

   Root Cause: The critical logic within the HD interface block that generates the unsolicited response does not have BITCLK available during link shutdown and therefore fails to register the triggering edge.

   Workaround: To clear any potential pending UR event, the driver should manually issue a Get Pin Sense verb to all four pin complexes that are Presence Detect Capable (PDC; that is, Node ID = [09h, 0Dh, 0Ch, 0Ah]) when the controller resumes from D3 aisnd the link is reactivated. Reading the Pin Sense status clears any pending UR events and prevents the codec from issuing another power state change request.

   Resolution: None. Use software workaround.

2. If unsolicited responses for the S/PDIF Rx Input Pin Widget (NID = 0Fh) are disabled (URE = 0b), and the S/PDIF Rx Input Converter Widget (NID = 07h) is powered up (PS-Act = 0h), and a change in the S/PDIF Rx Lock Status occurs, any widgets that are Presence Detect Capable (PDC) (that is Node ID = [09h, 0Dh, 0Ch, 0Ah]) no longer generate unsolicited responses.

   Root Cause: The S/PDIF Rx uses the lock signal as a plug-in event for unsolicited response. Even if unsolicited responses are disabled, the jack sense latching block still puts the lock signal into the processing queue, but it never gets processed since URs are disabled. Therefore, this event remains in the queue indefinitely and is blocking all subsequent jack sense unsolicited responses.

   Workaround: To prevent this problem, enable unsolicited responses for the S/PDIF Rx Input Pin Widget (URE = 1b) before powering up the S/PDIF Rx Input Converter Widget. To reenable unsolicited responses after the problem has already occurred, power down the S/PDIF Rx Input Converter Widget, enable unsolicited responses for the S/PDIF Rx Input Pin Widget, and then power up the S/PDIF Rx Input Converter Widget.

   If the driver is not designed to handle (or does not expect) unsolicited responses from the S/PDIF Rx, be careful in your choice of the Tag field for the Unsolicited Response control. If you choose a unique tag, the driver may disregard the UR, but it may also become confused by a tag value that it is unable to associate with a widget. If you choose a tag that has already been assigned, the driver may draw the wrong conclusion if it automatically assumes that a Presence Detect status change occurred in another widget associated with

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that tag, without first reading the Pin Sense control. However, if the driver uses the UR simply as a trigger to read the Pin Sense control of the associated widget, it would see that no Presence Detect status change occurred and the latter method would be preferable.

Resolution: None. Use software workaround.

3. If MICBIAS is enabled (VREFE (NID = 0Dh) = [001b, 010b, 100b]), the ADC1/2 Input Converter Widgets (NID = 05h/06h) and the Line In/Mic In Pin Widgets (NID = 0Ch/0Dh) cannot be powered down, i.e., when PS-Act = 0h for any of these widgets, writing PS-Set = 3h still results in PS-Act = 0h.

   Root Cause: The ADC power control state machine checks the status of MICBIAS and only goes into full power-down state (PS-Act = 3h) when MICBIAS is disabled. Otherwise, it stays at an intermediate state and reports a PS-Act of 0h (D0) to the host. However, at this state, most of the ADC analog section is already powered down and therefore the total ADC current is very small.

   Workaround: Before transitioning any of the four affected widgets from D0 to D3, MICBIAS must be disabled (VREFE (NID = 0Dh) = 000b). MICBIAS may be reenabled after transitioning the widget(s) to D3, if desired.

   Resolution: None. Use software workaround.

4. If a DAC channel is unmuted (AM (NID = [02h, 03h, 04h]) = 0) and zero-cross is enabled on the same DAC (SZCMode = [01b, 11b]), that DAC cannot be powered down, i.e., when PS-Act = 0h, writing PS-Set = 3h still results in PS-Act = 0h.

   Root Cause: When setting PS-Set = 3h, a series of events is started to gracefully power down the DAC and output amplifiers without popping. One of those steps (which gates the PS-Act bit) is ramping the digital volume from its current setting to full attenuation. If zero-cross is enabled (either by itself or in conjunction with soft-ramp), any volume changes are held off, pending a polarity change of the signal. If no signal is present, a timeout counter triggers the volume change instead. However, the timeout counter never trips, because each timeout counter enable signal is gated with the corresponding PS-Set bit. Hence, the power-down sequence never completes, and PS-Act never reflects D3.

   Workaround: Before transitioning any of the DAC converter widgets from D0 to D3, ensure zero-cross is disabled (SZCMode = [00b, 10b]) for that DAC. Zero-cross may be reenabled after transitioning the widget to D3, if desired.

   Resolution: None. Use software workaround.

5. **For silicon revision C0 and C1 only:** If VD and VL_IF ramp up at the same time, or VL_IF ramps up before VD, there may be spurious glitches on the output pins in the VL_IF domain (SPDIF_OUT1, DMIC_SCL, GPIO0/DMIC_SDA1, GPIO1/DMIC_SDA2/SPDIF_OUT2, GPIO2, GPIO3) until VD has stabilized.

   Root Cause: The level shifters that connect each of those pins to the digital core (which is on the VD domain) are supposed to be held in reset until the digital supply VD has stabilized and the digital core has properly initialized. However, this reset signal is incorrectly tied to VL_IF, which means the level shifters come out of reset as soon as VL_IF reaches a certain threshold, regardless of whether the VD supply is stable and the digital core has been initialized or not. If VL_IF ramps up before VD is stable, the level shifters come out of reset while the digital core is in an uninitialized and unpredictable state, resulting in possible glitching on the outputs.

   Workaround: Ramp up VL_IF only after VD has stabilized or gate outputs in the VL_IF domain at the board level.

   Resolution: None. Use hardware workaround.

   For silicon revision C2 only: This issue was resolved by holding the level shifters for the output pins on the VL_IF domain in reset until VD has stabilized. There is no glitching on those outputs, regardless of which supply comes up first.

6. At high temperature (T_A > +85°C), the digital supply current (I_{VD}) may be excessive (up to an additional 200 µA), which is most easily observed while the part is being held in reset (RESET# active low).

Root Cause: At initial power up of the device, the logic that drives the clock and write enable to the S/PDIF SRC RAMs is not properly initialized. Certain random patterns cause a steady leakage current in those RAM cells. The issue is resolved when SRCs are used (turned on).

Workaround: The following verb sequence briefly turns on the S/PDIF SRC blocks, which alleviates the issue.

Verb	NID	VID	PL	Comment
x0170500	01h	705h	00h	AFG: D0
x1170301	11h	703h	01h	VPW: processing on
x1150008	11h	5h	0008h	VPW: coefficient index = 8h
x1149999	11h	4h	9999h	VPW: coefficient value = 9999h
x1150017	11h	5h	0017h	VPW: coefficient index = 17h
x114A412	11h	4h	A412h	VPW: coefficient value = A412h
x1150001	11h	5h	0001h	VPW: coefficient index = 1h
x1140009	11h	4h	0009h	VPW: coefficient value = 9h
x0770500	07h	705h	00h	S/PDIF Rx: D0
x0870500	08h	705h	00h	S/PDIF Tx: D0
x1150017	11h	5h	0017h	VPW: coefficient index = 17h
x1142412	11h	4h	2412h	VPW: coefficient value = 2412h
x1150008	11h	5h	0008h	VPW: coefficient index = 8h
x1140000	11h	4h	0000h	VPW: coefficient value = 0h
x1150001	11h	5h	0001h	VPW: coefficient index = 1h
x1140008	11h	4h	0008h	VPW: coefficient value = 8h
x1170300	11h	703h	00h	VPW: processing off
x0770503	07h	705h	03h	S/PDIF Rx: D3
x0870503	08h	705h	03h	S/PDIF Tx: D3
x0170503	01h	705h	03h	AFG: D3

The ‘x’ nibble at the beginning of each verb must be replaced with the proper codec address (CAd) for that particular system.

There is no side effect to executing this verb sequence, since any changes to the power-up defaults are restored. Furthermore, there are no timing constraints with this sequence. All verbs can be sent in consecutive frames, but it is not required to do so.

Resolution: None. Use software workaround.

- Cirrus Logic-supplied production drivers for Windows XP® and Windows Vista®/Windows 7™ released after July 2010 have been updated to include this verb sequence.
- Customers providing their own second- or third-party sourced drivers are strongly encouraged to incorporate the above outlined verb sequence into their codec initialization routine. This verb sequence must be sent every time the digital power supply is cycled, i.e., upon driver init, as well as when returning from a system-wide low-power state that removes the digital power supply from the codec. Although it is not required, there is no harm in executing this verb sequence when returning from a system-wide low-power state that puts the codec in D3 and/or asserts the RESET# signal, but doesn’t remove the digital power supply from the codec.

7. While the RESET# pin is low, the MICBIAS pin is in the high-impedance state. When the RESET# pin becomes high, the MICBIAS pin returns to the state indicated by the VREFE bits. This high-impedance state violates Section 7.3.3.10 of the HDA Specification 1.0a, which states that all fields in the Pin Widget Control should persist across an HDA link reset event.

   Root Cause: The MICBIAS control signals connecting digital to analog are low while a link reset occurs. When the control signals are in this state, the MICBIAS pin becomes high impedance.

   Workaround: The HDA link should not be reset (RESET# pin low) in order to prevent the MICBIAS pin from becoming high impedance.

   Resolution: None. Use hardware workaround.

2. PERFORMANCE DEVIATIONS

8. Max. V_{IL} for RESET# at VL_HD = 1.5 V is 0.20 • VL_HD.
9. Min. V_{IH} for RESET# at VL_HD = 1.5 V is 0.65 • VL_HD.
10. Max. V_{IL} for SDO, BITCLK, SDI, and SYNC at VL_HD = 1.5 V is 0.35 • VL_HD.