USB3-Gigabit Ethernet Demo

User Guide

FPGA-UG-02054-1.0

May 2018

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
EVDK	Embedded Vision Development Kit
USB	Universal Serial Bus
GbE	Gigabit Ethernet
I2C	Inter-Integrated Circuit
LDO	Low Dropout
LED	Light-emitting Diode
LVDS	Low-Voltage Differential Signaling
SPI	Serial Peripheral Interface
VIP	Video Interface Platform

1. Introduction

This document describes the design and setup procedure for the Lattice Embedded Vision Development Kit (EVDK) and the USB3-GbE VIP IO Board to demonstrate USB3 and GigE video streaming via USB3 or GigE network connection. The EVDK and the USB3-GbE VIP IO Board are members of Lattice's Video Interface Platform (VIP).

1.1. Hardware Requirements

1.1.1. EVDK

Figure 1.1 and Figure 1.2 show the Embedded Vision Development Kit board configuration, which is designed as a stackable modular architecture with 80 mm × 80 mm form factor. The Embedded Vision Development Kit consists of three boards:

- CrossLink™ Video Interface Platform (VIP) Input Bridge Board
- ECP5 VIP Processor Board
- HDMI VIP Output Bridge Board

The figures shown in this document are part of Revision C of the Embedded Vision Development Kit. For earlier versions, refer to the individual evaluation board's user guide. For more information on the Embedded Vision Development Kit, visit www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/EmbeddedVisionDevelopmentKit.aspx.

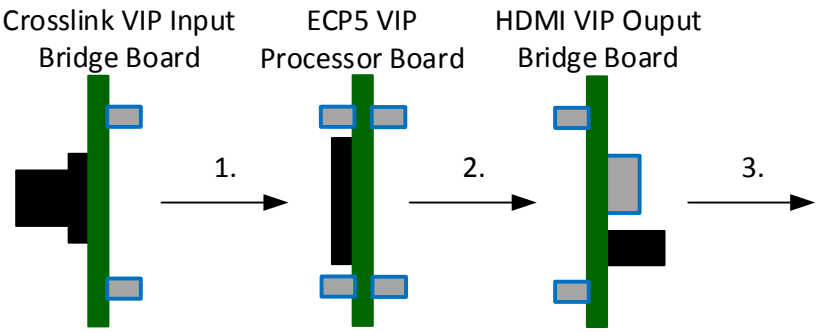

Figure 1.1. EVDK Default Board Configuration

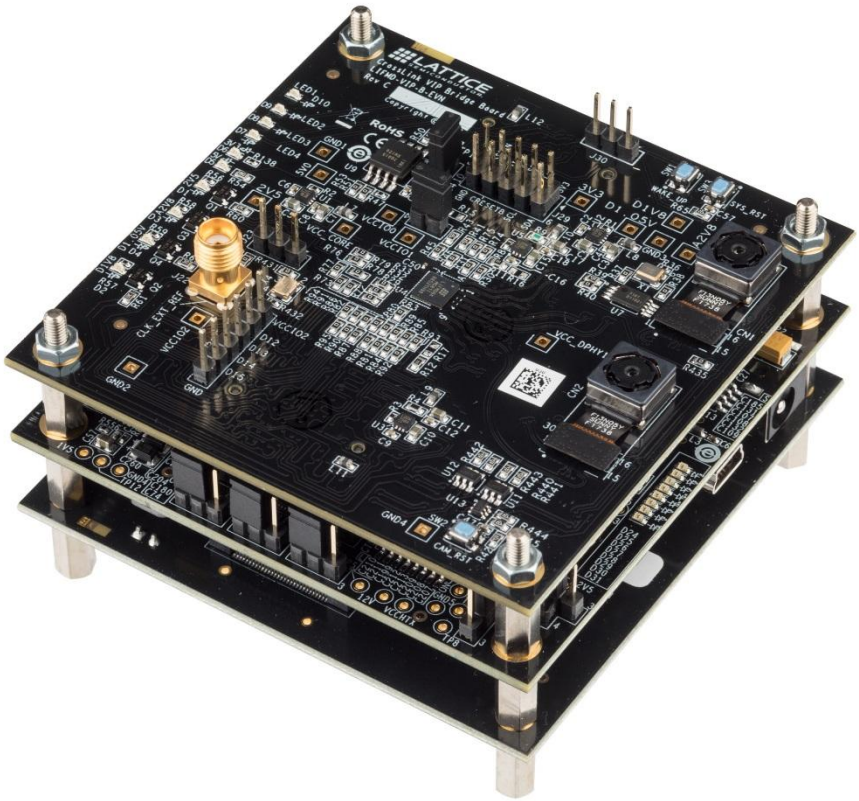

Figure 1.2. Embedded Vision Development Kit

1.1.2. USB3-GbE VIP IO Board

In addition to the Embedded Vision Development Kit, the following items are required to demonstrate USB3 and GigE video streaming:

- USB3-GbE VIP IO Board
- Ethernet cable
- USB3 Type A to Micro-B cable

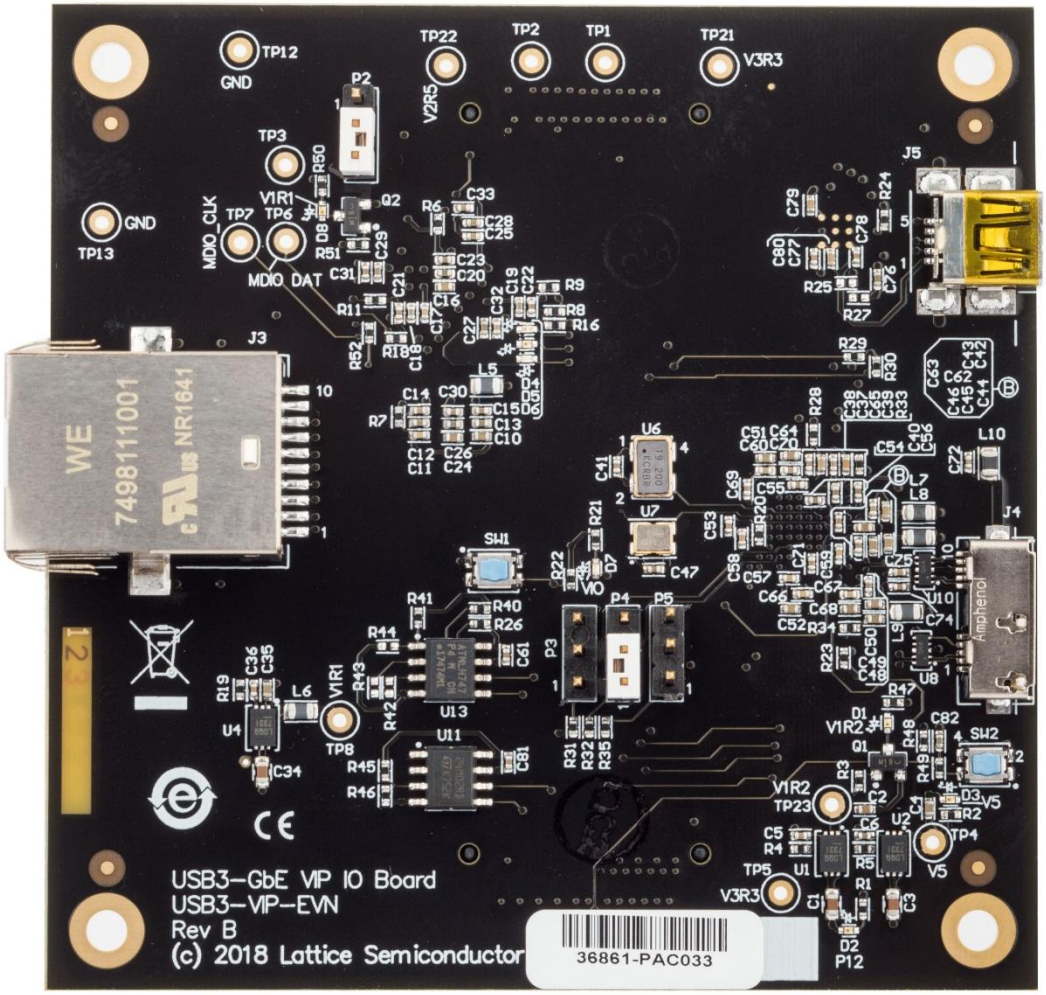

Figure 1.3. USB3-GbE VIP IO Board Rev. B

1.2. Software Requirements

Before proceeding with the demo board setup, download the following software:

- Lattice Diamond Software
- Video player:
  - Gstreamer (or any RTP Video Player):
    https://gstreamer.freedesktop.org/pkg/windows/1.14.0.1/gstreamer-1.0-x86_64-1.14.0.1.msi
  - AmCap (or any UVC viewer)
    https://amcap.en.softonic.com
- Cypress EZ-USB FX3 Software Development Kit (SDK):
  www.cypress.com/documentation/software-and-drivers/ez-usb-fx3-software-development-kit

  Note: This is optional as the USB3-GigE VIP IO Board is pre-loaded with the FX3 Firmware.

2. Demo Board Setup

To perform the USB3 and GigE video streaming demo, replace the HDMI VIP Output Bridge Board with the USB3-GbE VIP IO Board, as shown in Figure 2.1.

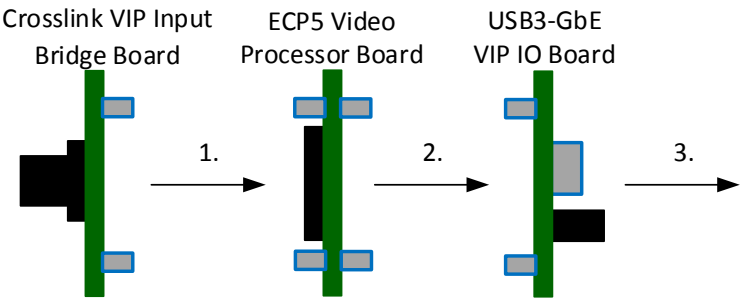

Figure 2.1. Required Board Configuration for the USB3 and GigE Video Streaming Demo

To obtain the required board configuration:

1. It is recommended to erase the Flash on ECP5 Board before proceeding.
    a) Erase ECP5 Device
    b) Erase SPI Flash
2. Remove power from the EVDK.
3. Remove the HDMI VIP Output Bridge Board.
4. Install the USB3-GbE VIP IO Board.
    a) Connect J1 (60-pin) connector to J12 of the ECP5 VIP Processor Board.
    b) Connect J2 (60-pin) connector to J13 of the ECP5 VIP Processor Board.

3. Configuring and Running the USB3 and GigE Video Streaming Demo

The USB3 and GigE video streaming demo consists of two independent parts, which requires two separate bit-streams for the ECP5 FPGA. Each of these demos has its own bit-stream file, and only allows to operate one interface at a time. It is assumed that the Crosslink device is programmed with Dual CSI-2 Camera to HDMI Bridge Demo, which is pre-loaded by default. The Crosslink bit stream is common for both demos.

- Demo_USB3_A.bit – Bit stream file for the USB3 video streaming via USB2 UVC.
- GbE_A.bit – Bit stream file for the GigE video streaming via GigE network connection.

The following sections describe each demo independently.

3.1. Configuring and Running the USB3 Demo

3.1.1. Configure the USB3 Demo

To configure the USB3 Demo:

1. Ensure that you have a video viewer installed on your PC which supports USB UVC streaming. This demo uses AMCap, which is a Windows based video capture software. Any other software supporting USB UVC can be used.
2. To allow booting from I^2C, power OFF the USB3-GbE VIP IO board and set the jumpers as shown in Figure 3.1.

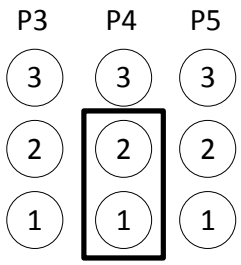

Figure 3.1. Jumper Setting for I^2C Booting

3. Power ON the board.
4. Using the USB 3.0 Type A to Micro-B cable, connect the Micro-B connector (J4) on the USB3-GbE VIP IO board to your PC USB 3.0 (Type-A) port.
5. Ensure that the USB firmware is already loaded on the FX3 USB controller.
    a) Press SYS_RST (SW3) on CrossLink Board.
    b) Under Device Manager -> Imaging Devices, FX3 should be detected.

    For more details on how to download the USB firmware to the FX3 USB controller, see Appendix B.
6. Program ECP5 with the **Demo_USB3_A.bit** bit stream file into the ECP5 SPI Flash. For details on how to program the ECP5, see Appendix A.

3.1.2. Run the USB3 Demo

To run the USB3 demo:

1. Power cycle the EVDK.
2. Press the Reset button on the CrossLink board (SW3).
3. Run AMCap.
4. Under Devices, select FX3.
5. Under Options, select Preview.
6. The video image will be displayed.

3.2. Configuring and Running the GigE Demo

3.2.1. Configuring the GigE Demo

To configure the GigE demo:

1. Ensure that you have a video viewer installed on your PC which supports RTP video streaming. This demo uses Gstreamer, which is a Windows based video capture software. Any other software supporting RTP video streaming can be used.
2. Ensure that power is connected to the board.
3. Configure the network parameters of the destination PC with static IP address of 192.168.0.109 and subnet mask 255.255.255.0, as described in Appendix C. The default source IP address of the USB3-GigE VIP IO Board is hard coded in the RTL code to 192.168.0.11.

   Note: It is recommended to write down your original settings so you can restore your PC to its normal settings afterward.
4. Program the ECP5 with the GbE_A.bit bit stream into the ECP5 SPI Flash. For details on how to program ECP5, see Appendix A.
5. Connect the Ethernet cable between the USB3-GigE VIP IO Board and the PC.

3.2.2. Running the GigE Demo

To run the GigE demo:

1. Power cycle the EVDK.
2. Press the Reset button on the CrossLink board (SW3).
3. On a Windows PC, run Command Prompt (cmd.exe).
4. Change into the Gstream directory with the executable file. For example, cd gstream\1.0\x86_64\bin.
5. Run Gstreamer to display the RTP video. The RTP stream is point to point over UDP port 40963 with a target of 1920x1080p. The bit rate is around 900Mb/s over Ethernet to provide a frame rate a bit above 26fps.
   From the command line, enter:

```
>>gst-launch-1.0 udpsrc port=40963 caps="application/x-rtp,
sampling=(string)YCbCr-4:2:2, width=(string)1920, height=(string)1080" !
rtpvrawdepay ! autovideosink
```

6. The video image is displayed as shown in Figure 3.2.

Figure 3.2. Resulting Video Image

Appendix A.
Programming the Lattice Embedded Vision Development Kit

Using Diamond Programmer with the EVDK

The EVDK has a built in download controller for programming. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download controller, connect the USB cable from J2 of the ECP5 VIP Processor Board to your PC (with Diamond programming software installed). A mini USB to USB-A cable is included in the EVDK. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in download controller available for use with the Diamond programming software.

In order to provide a single programming interface for the EVDK, the ECP5 VIP Processor Board's JTAG interface is shared with the CrossLink VIP Input Bridge Board's SPI programming interface. During a JTAG scan, the Diamond Programmer will only see one of the devices:

- LFE5UM-85F, if the CrossLink device is currently programmed
- LIF-MD6000, if the CrossLink device is not programmed

A JTAG scan also erases both ECP5 and CrossLink SRAM images, requiring you to reprogram both devices. When using the Diamond Programmer, selecting **Create a new blank project** and manually selecting the device family and device prevents the erasure of both devices.

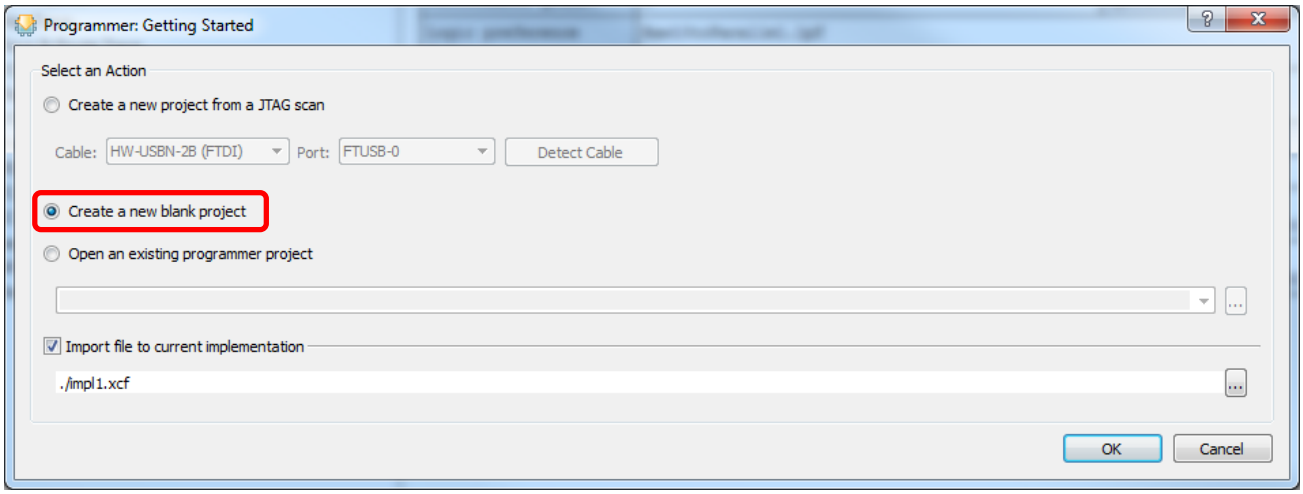

Figure A.1. Create a New Blank Project

ECP5 SPI Flash Programming

Erasing the ECP5 Prior to Reprogramming

If the ECP5 is already programmed (either directly, or loaded from SPI Flash), erase first the ECP5 SRAM memory, then program the ECP5's SPI Flash in the next section. Keep the board powered when re-programming the SPI Flash in the next section.

To erase the ECP5:

1. Launch Diamond Programmer with **Create a new blank project.**
2. Select **ECP5UM** for **Device Family** and **LFE5UM-85F** for **Device**.

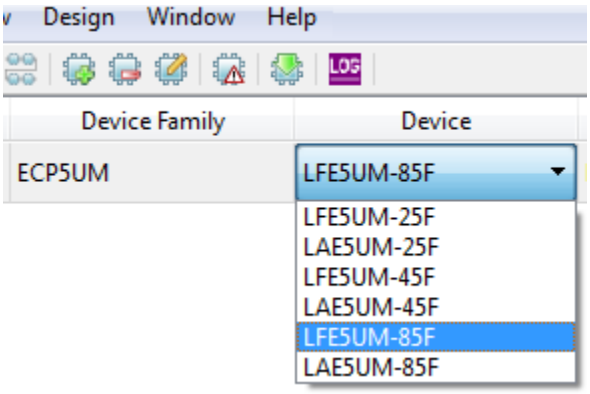

Figure A.2. Selecting Device

3. Right-click and select **Device Properties**.
4. Select **JTAG 1532 Mode** for **Access Mode** and **Erase Only** for **Operation**.

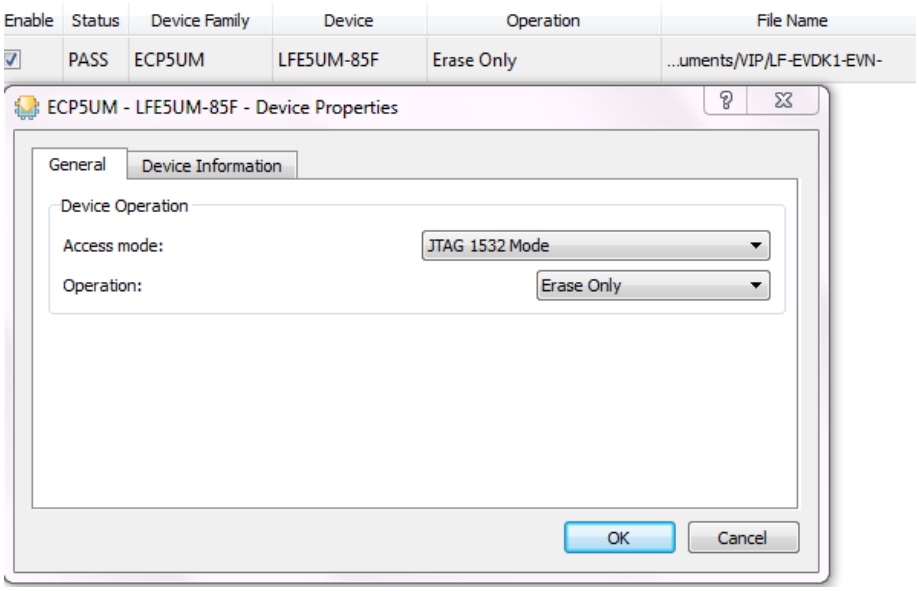

Figure A.3. Device Operation

5. Click **OK** to close the Device Properties window.
6. Click the **Program** button  in Diamond Programmer to start the Erase sequence.

Programming the SPI on the ECP5 VIP Processor Board

To program the SPI:

1. Ensure the ECP5 device is erased by performing Steps 1-6.
2. Right-click and select **Device Properties**.
3. Select **SPI Flash Background Programming** for **Access mode** and make the following selections:
    a) For **Programming File**, browse and select the ECP5 bit file (*.bit).
    b) For **SPI Flash Options**, refer to the table below.

Table A.1. SPI Flash Options Selection Guide

Item	Rev A/B	Rev C
Family	SPI Serial Flash	SPI Serial Flash
Vendor	Micron	Macronix
Device	SPI-N25Q128A	MX25L12805

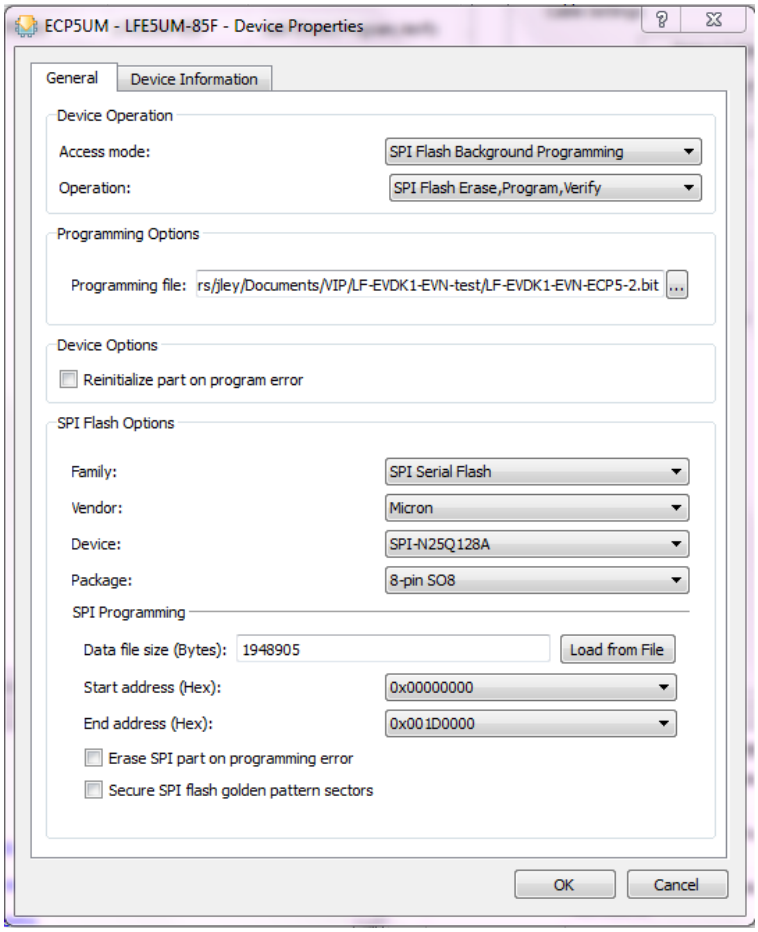

Figure A.4. Device Properties

4. Click **OK** to close the Device Properties window.
5. Click the **Program** button  in Diamond Programmer to start the programming sequence.
6. After successful programming, the Output console displays the results as shown in Figure A.5.

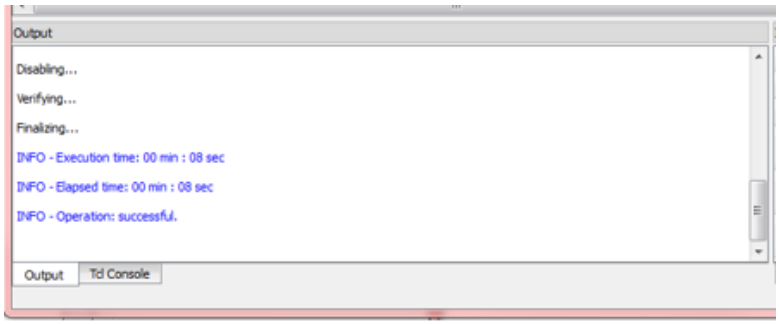

Figure A.5. Output Console

CrossLink SPI Flash Programming

Erasing the CrossLink FPGA Prior to Reprogramming

If the CrossLink is already programmed (either directly, or loaded from SPI Flash), you'll need to follow this procedure to first erase the CrossLink SRAM memory before re-programming the CrossLink SPI Flash. If you are doing this, you need to keep the board powered when re-programming the SPI Flash (so it doesn't re-load on re-boot).

To erase CrossLink:

1. Launch Diamond Programmer with **Create a new blank project**.
2. Select **LIFMD** for **Device Family** and **LIF-MD6000** for **Device**.

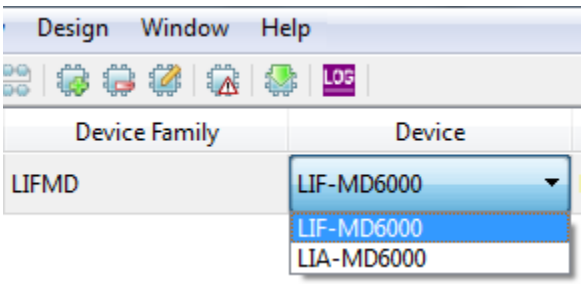

Figure A.6. Select Device

3. Right-click and select **Device Properties.**
4. Select SSPI SRAM Programming for Access Mode and Erase Only for Operation.

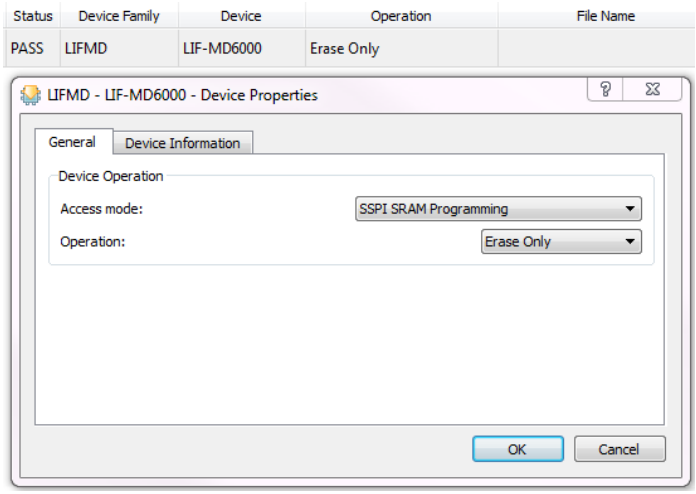

Figure A.7. Device Operation

5. Click **OK** to close the Device Properties window.
6. Click the **Program** button  in Diamond Programmer to start the Erase sequence.

Programming the SPI on the CrossLink VIP Input Bridge Board

To program the SPI:

1. Ensure the CrossLink device is erased by performing Steps 1-6.
2. Right-Click and select Device Properties.
3. Select SPI Flash Programming for Access mode and make the following selections:
   a. For Programming File, browse and select the CrossLink bit file (*.bit).
   b. For **SPI Flash Options**, refer to the table below.

Table A.2. SPI Flash Options Selection Guide

Item	Rev A/B	Rev C
Family	SPI Serial Flash	SPI Serial Flash Beta
Vendor	Micron	Micron
Device	SPI-M25PX16	SPI-MT25QL128A

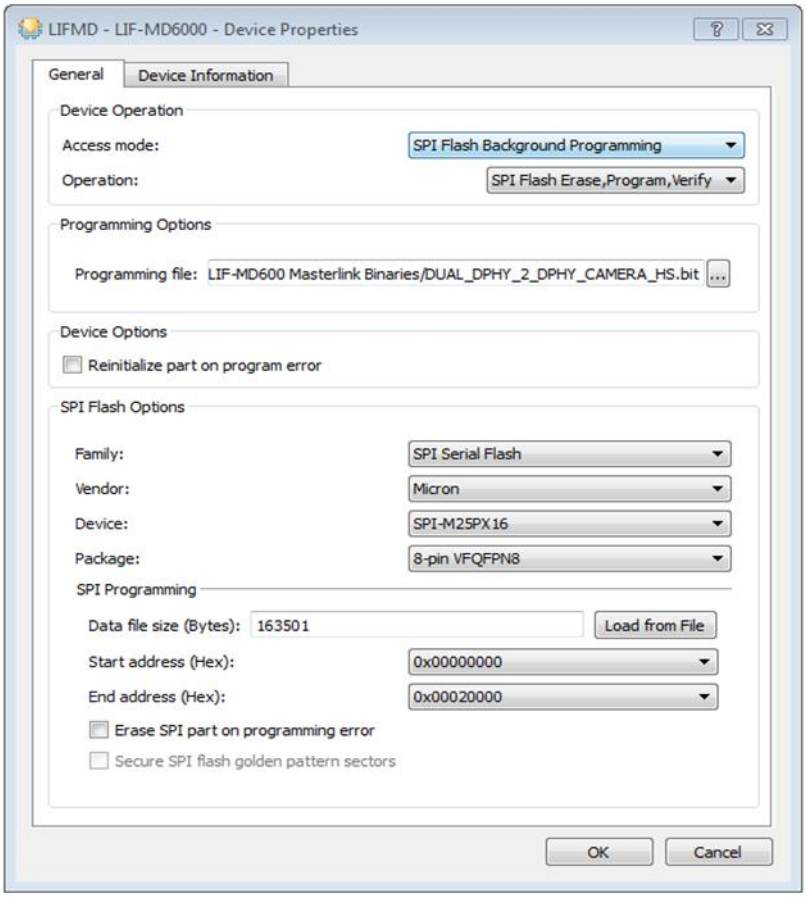

Figure A.8. Device Properties

4. Click **OK** to close the Device Properties window.
5. Click the **Program** button  in Diamond Programmer to start the programming sequence.
6. After successful programming, the Output console displays the results as shown in Figure A.9.

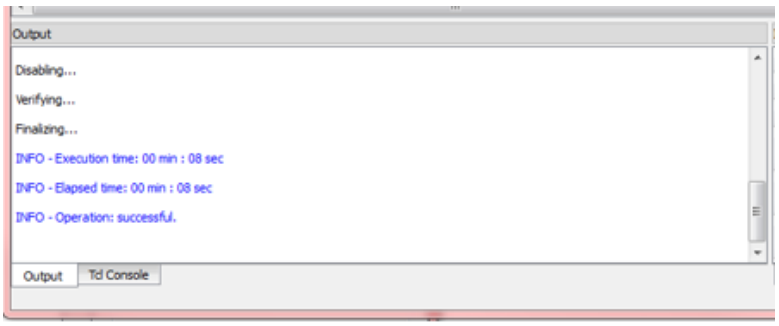

Figure A.9. Output Console

Appendix B.
Configuring the FX3 USB Controller

Before you configure the FX3 USB Controller, download and install the FX3 Software Development Kit (SDK) on your computer. The Cypress EZ-USB FX3 Software Development Kit (SDK) can be downloaded from the following link:

www.cypress.com/documentation/software-and-drivers/ez-usb-fx3-software-development-kit

Note: The FX3 Software only needs to be loaded once and remains in the FX3 USB Controller.

To configure the FX3 USB Controller:

1. Power OFF the USB3-GbE VIP IO board and set the jumpers for USB Boot as shown in Figure B.1.

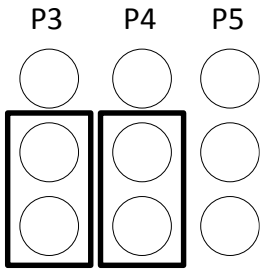

Figure B.1. Jumper Settings for USB Booting

2. Power ON the board.
3. Connect the Micro USB cable to the J4 connector of the USB3-GigE VIP IO board and the USB port of the PC.
4. Open the USB Control Center of the FX3 USB3 Controller SDK (All Programs->Cypress->EZ-USB FX3 SDK->Cypress USBSuite->Control Center).
5. Program the EEPROM with FX3 Image:
   a) Program -> FX3 -> I2C EEPROM
   b) Select **File** to download cyfxuvc.img

   Note: The cyfxuvc.img file is included in the compressed file USB3-GigE Demo Bit Stream available on the Lattice Semiconductor web site at http://www.latticesemi.com/Products/DevelopmentBoardsAndKits/USB3GBeVIPIOBoard.
6. You should be able to see the following information in Figure B.2 when your download is complete.

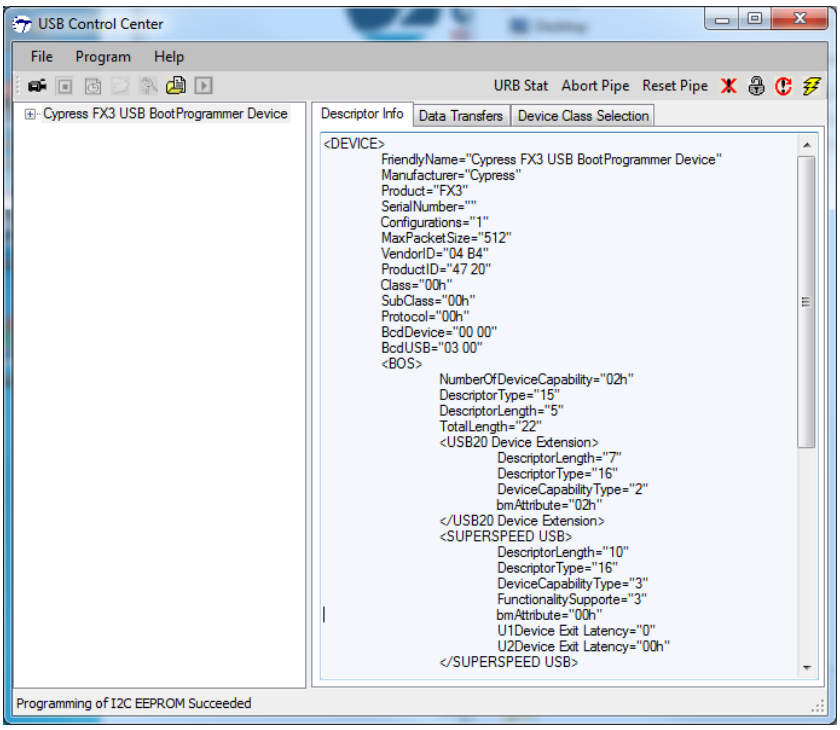

Figure B.2. USB Control Center Descriptor Info

Appendix C.
Changing Network Connection to Static IP Address

To change network connection to static IP address:

1. Select Control Panel > Network and Internet->Network Connections.
2. Disconnect Wireless Connection.
3. Right-click Local Area Connection and select Properties.
4. Select Internet Protocol Version 4 (TCP/IPv4), and then select Properties.

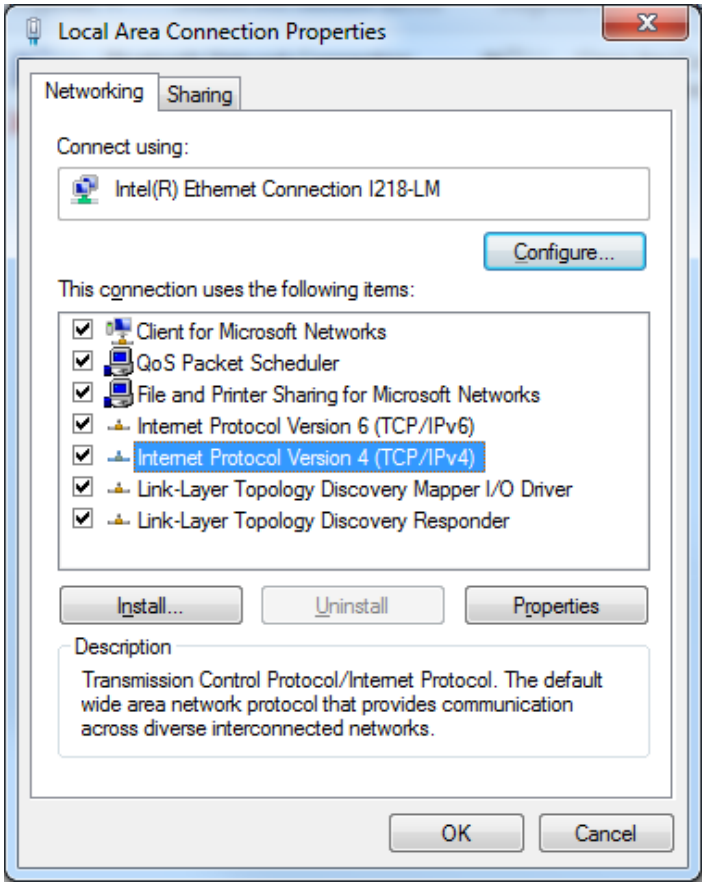

Figure C.1. Setting LAN Properties

5. Select **Use the following IP Address** and fill in the following:
   - IP Address: 192.168.0.109
   - Subnet mask: 255.255.255.0

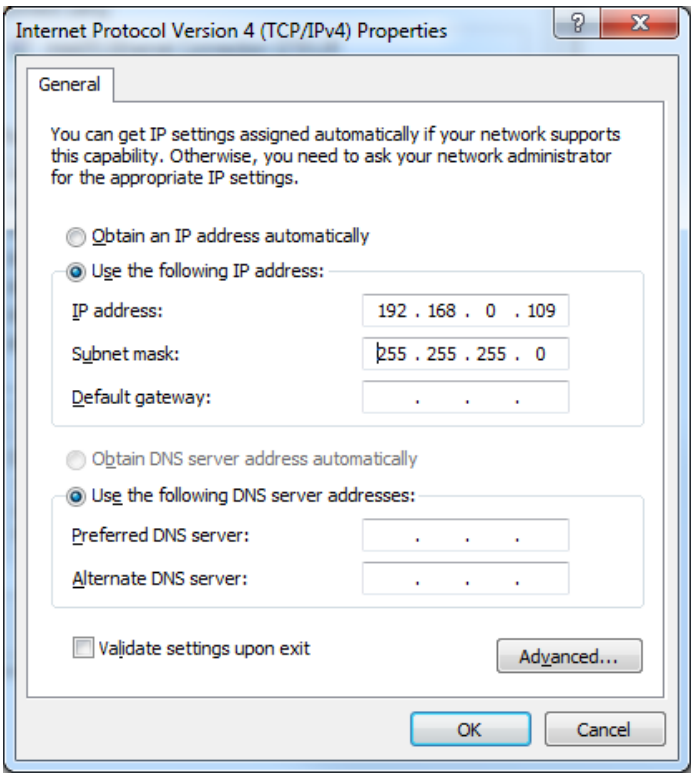

Figure C.2. Setting IP Address

6. Click **OK** to close Internet Protocol Properties window.
7. Click **Close** to close Local Area Connection Properties window.

Revision History

Date	Version	Change Summary
May 2018	1.0	Initial release.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com