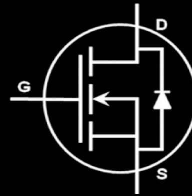
EPC2012C – Enhancement Mode Power Transistor

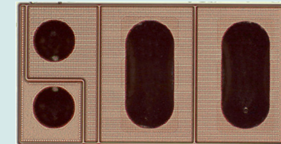
V_{DSS} , 200 V
$R_{DS(on)}$, 100 mΩ
I_D , 5 A

NEW PRODUCT



Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage	200	V
I_D	Continuous (T_A =25˚C, $R_{θJA}$ = 26)	5	A
	Pulsed (25˚C, T_{Pulse} = 300 µs)	22	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	



EPC2012C eGaN® FETs are supplied only in passivated die form with solder bars

Applications

- High Speed DC-DC conversion
- Class D Audio
- High Frequency Hard-Switching and Soft-Switching Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2012C.aspx

Static Characteristics (T_J= 25˚C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 60 µA	200			V
I_{DSS}	Drain Source Leakage	V_{DS} = 160 V, V_{GS} = 0 V		10	50	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.2	1	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		10	50	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 3 A		70	100	mΩ
Source-Drain Characteristics (T_J= 25˚C unless otherwise stated)						
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.9		V

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction to Case	4.2	˚C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	12.5	˚C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient (Note 1)	85	˚C/W

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J= 25˚C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance			100	140	
C_{OSS}	Output Capacitance	V_{GS} = 0 V, V_{DS} = 100 V		64	85	pF
C_{RSS}	Reverse Transfer Capacitance			0.4	0.6	
R_G	Gate Resistance			0.6		Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, I_D = 3 A, V_{GS} = 5 V		1	1.3	
Q_{GS}	Gate to Source Charge			0.3		
Q_{GD}	Gate to Drain Charge	V_{DS} = 100 V, I_D = 3 A		0.2	0.35	nC
$Q_{G(TH)}$	Gate Charge at Threshold			0.2		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 100 V		10	13	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

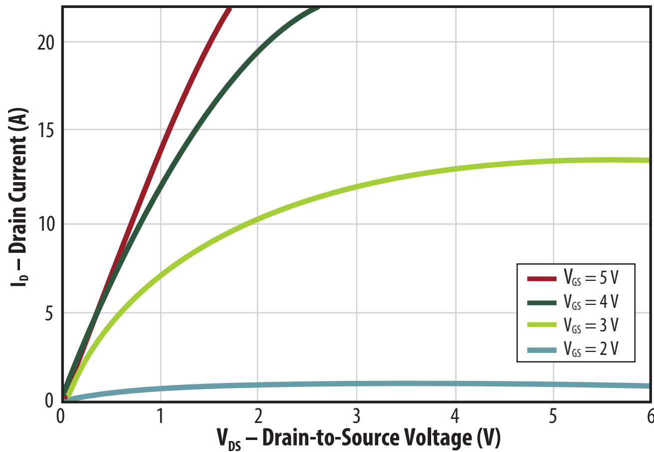


Figure 2: Transfer Characteristics

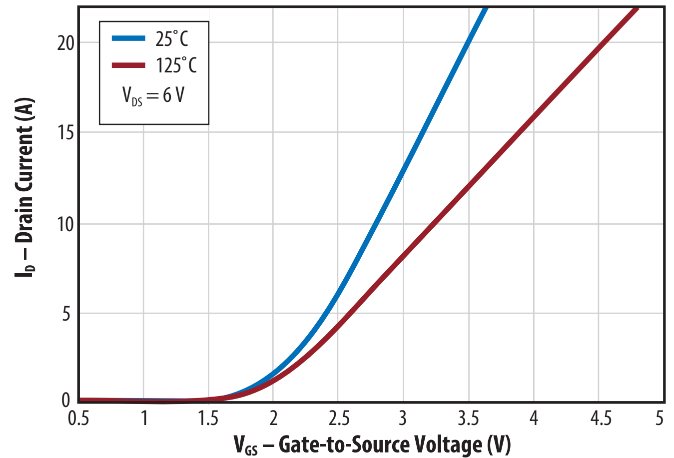


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

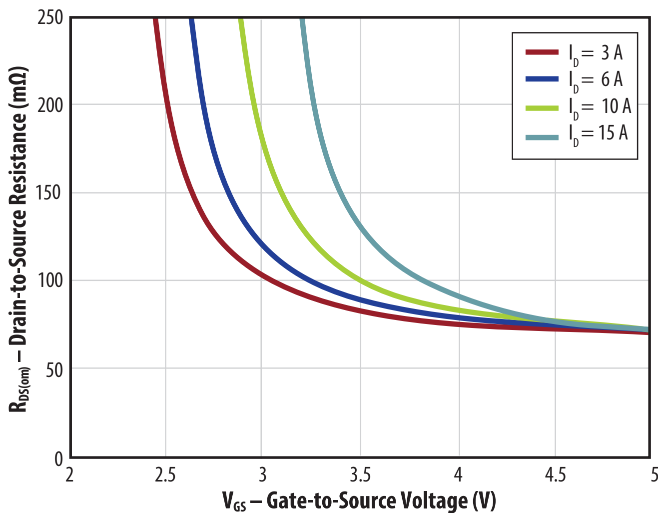
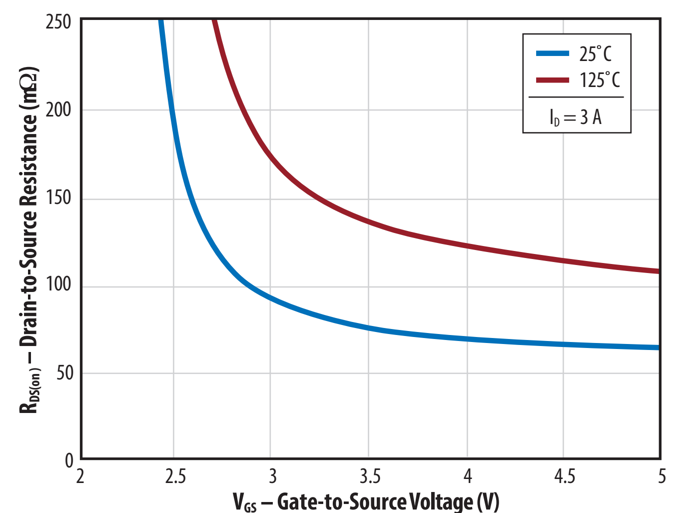
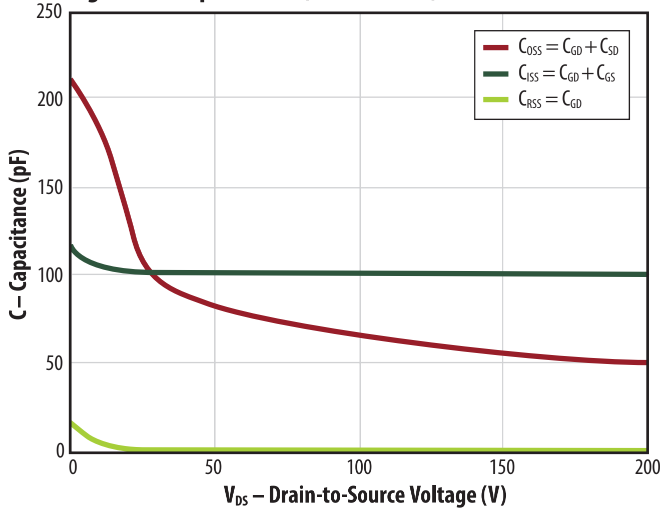
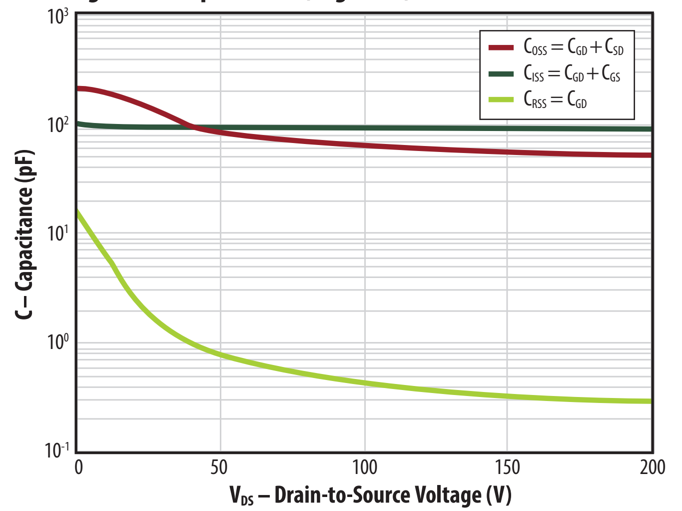
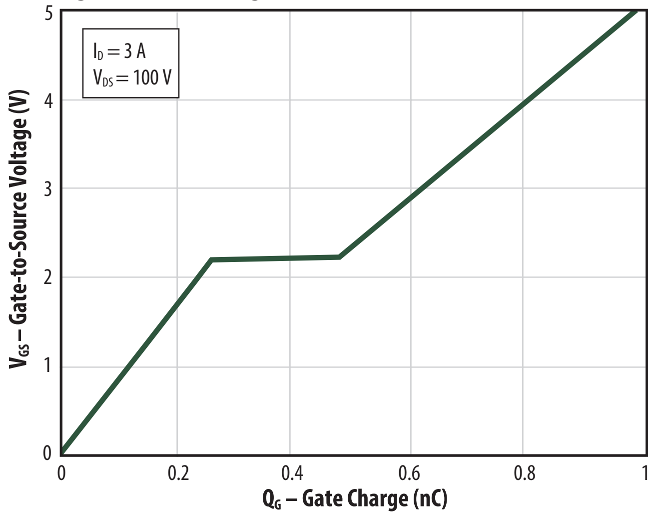


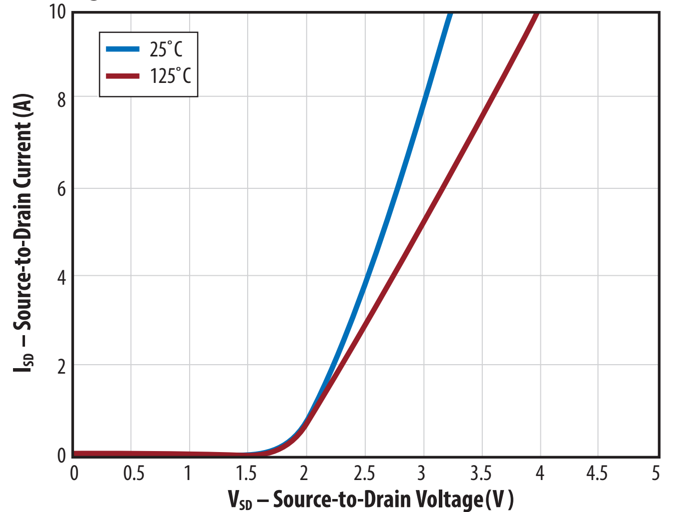
Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

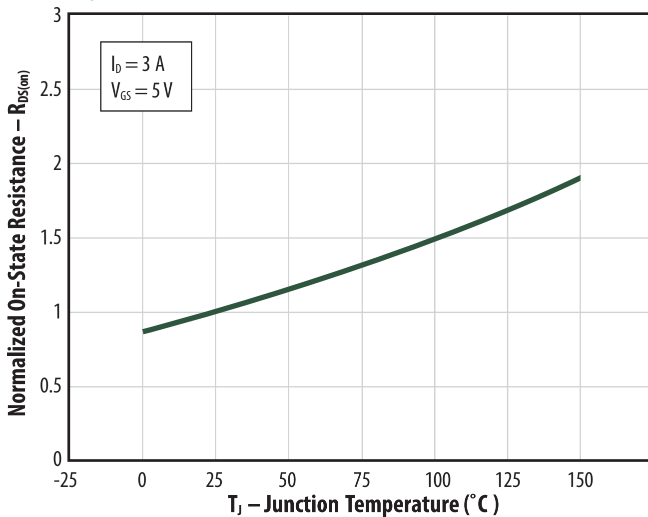


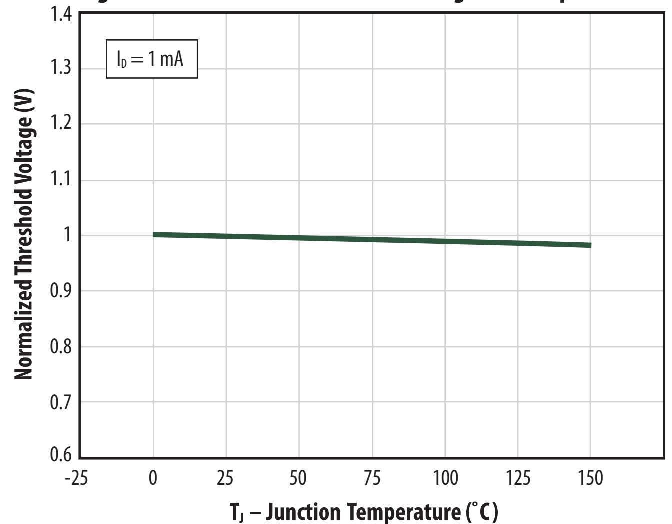












All measurements were done with substrate shortened to source.

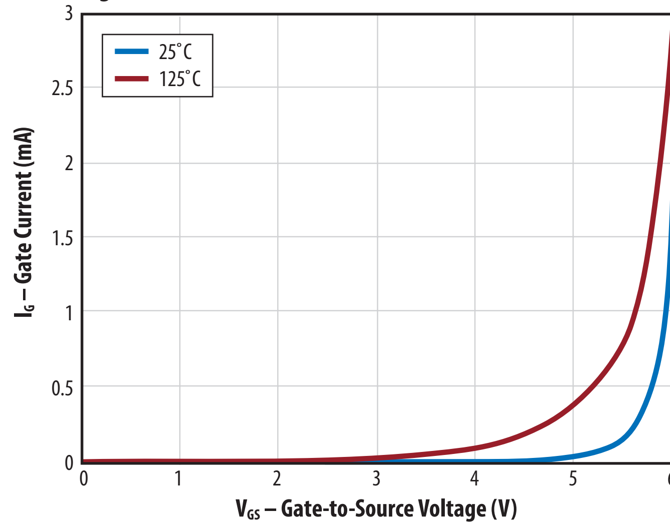


Figure 11: Transient Thermal Response Curves

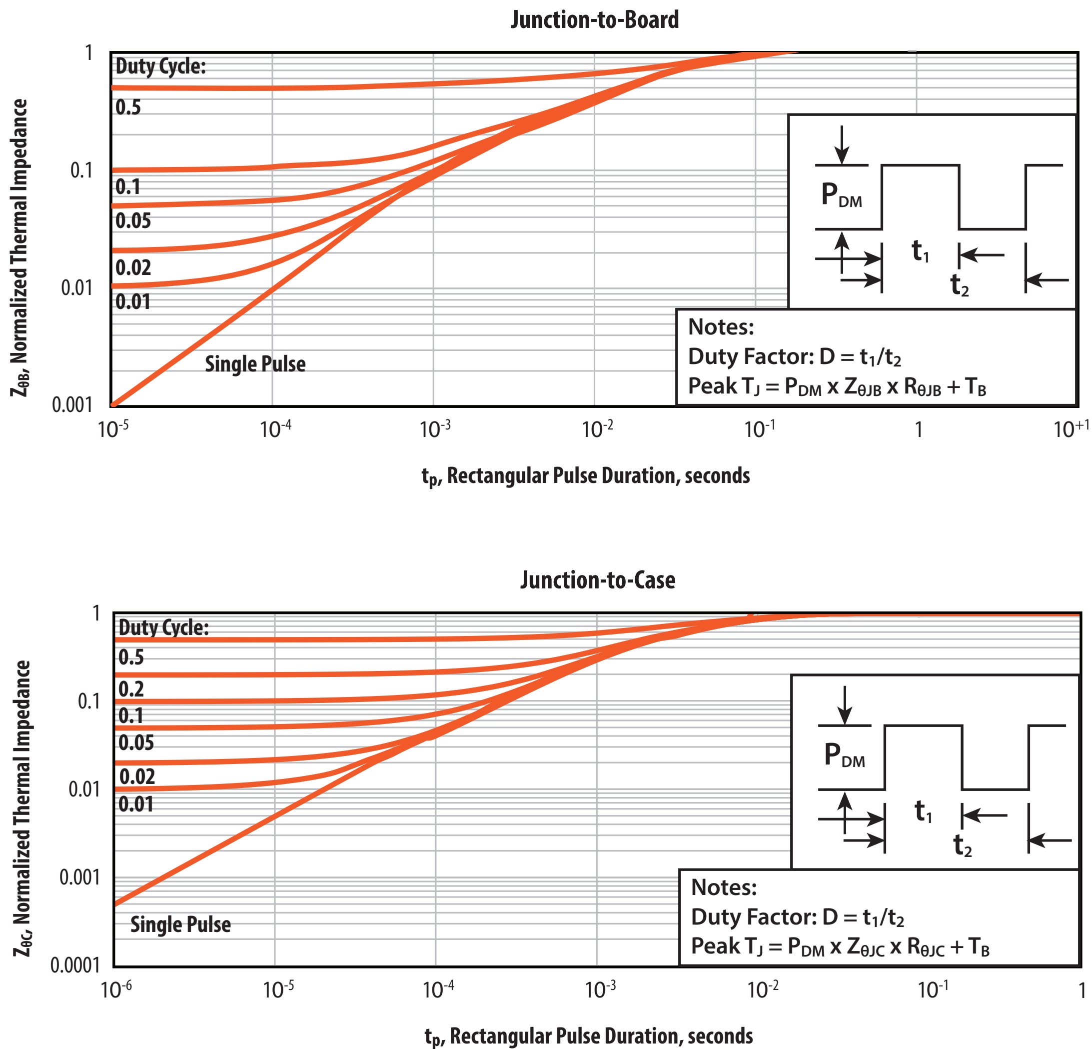
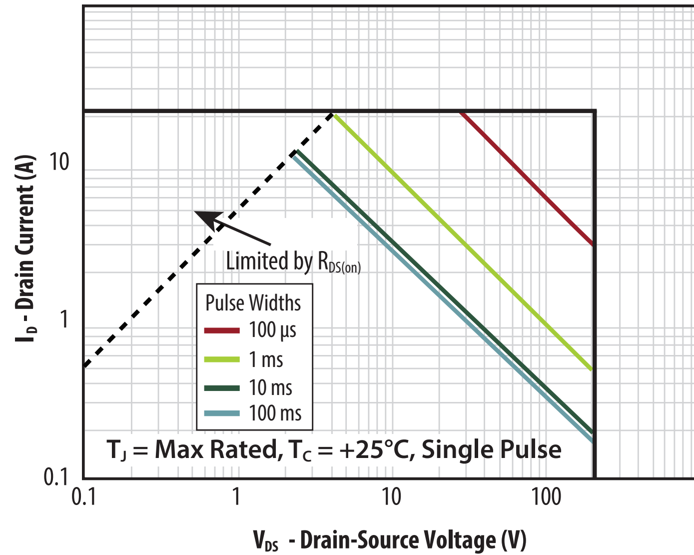
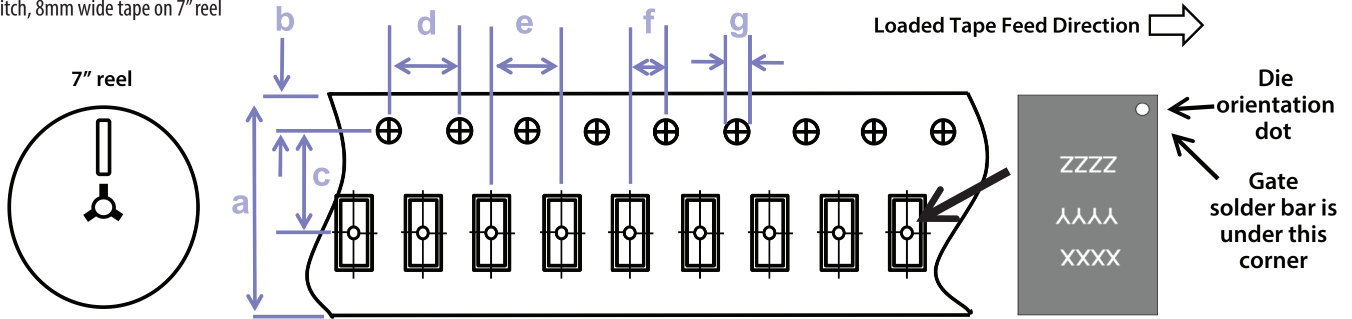


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

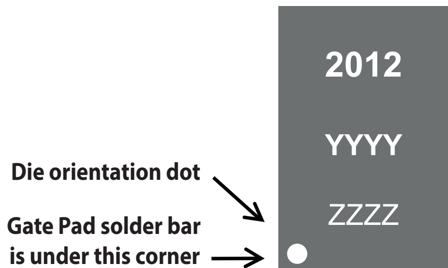


Die is placed into pocket solder bar side down (face side down)

	EPC2012C (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

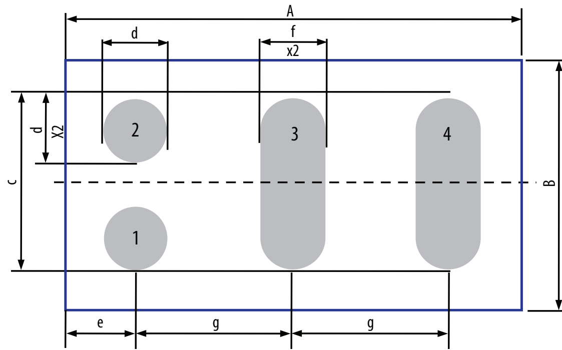
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2012C	2012	YYYY	ZZZZ

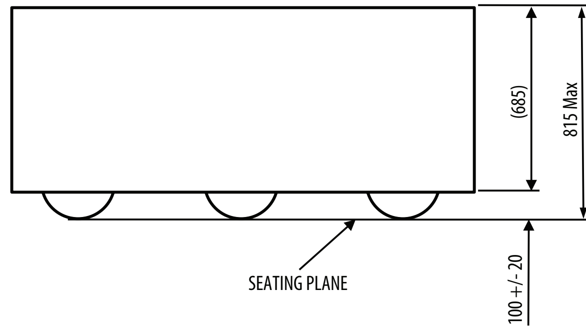
DIE OUTLINE

Solder Bar View



DIM	MILLIMETERS		
	MIN	Nominal	MAX
A	1.681	1.711	1.741
B	0.889	0.919	0.949
c	0.660	0.663	0.666
d	0.251	0.254	0.257
e	0.230	0.245	0.260
f	0.251	0.254	0.257
g	0.600	0.600	0.600

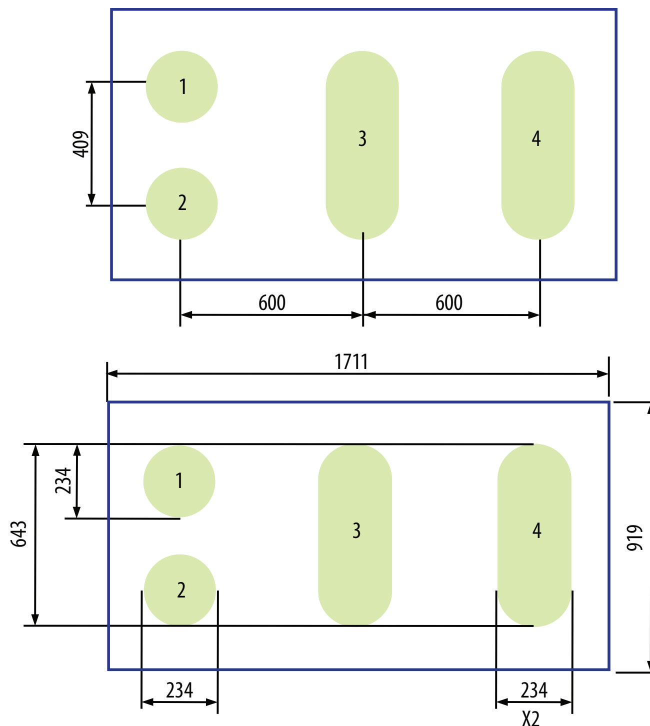
Side View



RECOMMENDED LAND PATTERN

(units in µm)

The land pattern is solder mask defined



3 4

Pad no. 1 is Gate

Pad no. 2 is Substrate

Pad no. 3 is Drain

Pad no. 4 is Source

For assembly recommendations please visit www.epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398

Information subject to change without notice.

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