# GS6081

## Gennum Products

## Features

- Supports data rates from 270Mb/s to 5.94Gb/s
- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 compliant
- Supports DVB-ASI at 270Mb/s
- Wide common-mode range input buffer
  - 100mV sensitivity
  - supports DC-coupling to industry-standard differential logic
  - on-chip 100Ω differential data input termination
- Input signal trace equalization
- Dual differential coaxial-cable-driving outputs
  - selectable slew rates
  - adjustable output swing from 500mV$_{pp}$ to 1040mV$_{pp}$
  - independent disable controls for each output
- Robust signal presence function
- Excellent output eye quality
- Power supply operation at +3.3V or +2.5V
- 135mW power consumption (+2.5V supply)
- Operating temperature range: -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
  - new dual-output pin out
  - use the GS6080 for a single-output variant that is drop-in compatible to the GS2988
- Pb-free and RoHS compliant

## Applications

- 6G UHD-SDI, SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 coaxial cable serial digital interfaces

## Description

The GS6081 is a high-speed BiCMOS integrated circuit designed to drive one to four 75Ω coaxial cables.

The GS6081 may drive data rates up to 5.94Gb/s and provides two selectable slew rates in order to achieve compliance to SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259.

The GS6081 accepts industry-standard differential input levels including LVPECL and CML.

Input trace equalization compensates for up to 10 inches of FR4 trace loss while in HD, 3G and UHD modes. This feature is enabled and disabled using the $\overline{\text{EQ\_EN}}$ pin.

The $\overline{\text{DISABLE1}}$ and $\overline{\text{DISABLE2}}$ pins power-down the first and second output drivers respectively, leaving the serial data outputs in a high-impedance state. When applied simultaneously, the entire device is powered-down.

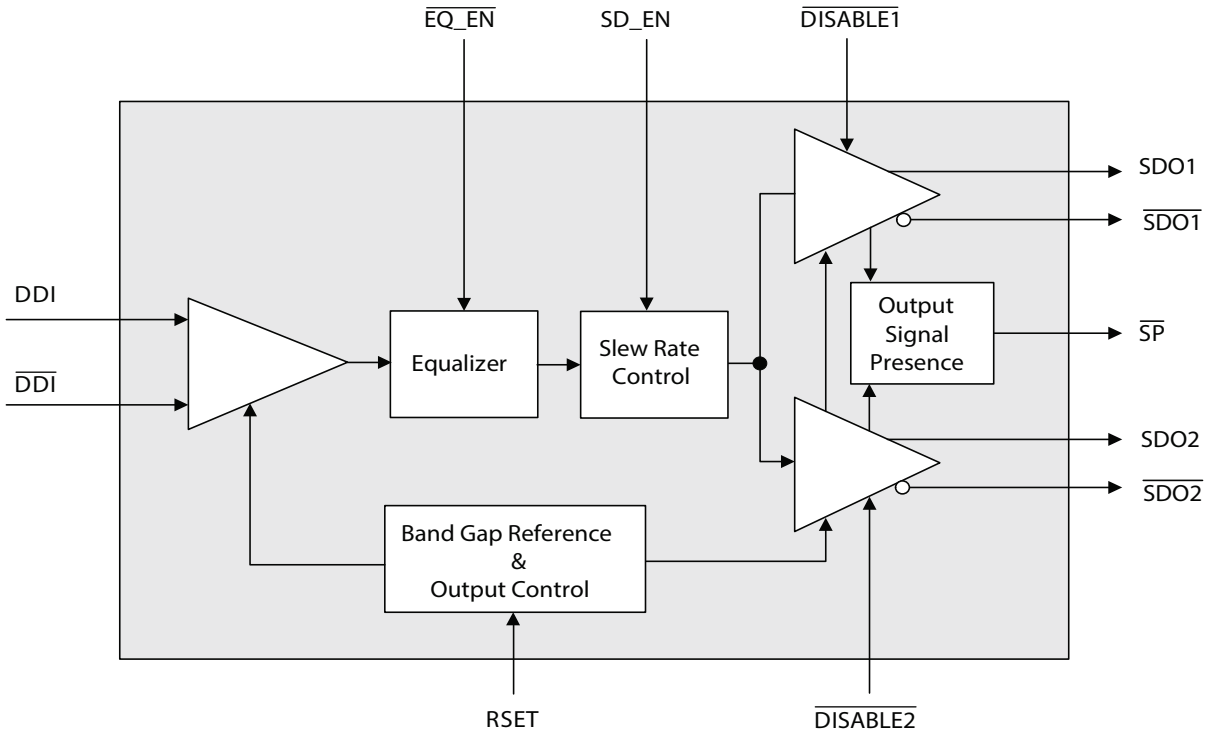
The GS6081 features adjustable output swing using an external bias resistor. The single-ended output swing is adjustable from 500mV$_{pp}$ to 1040mV$_{pp}$.

An output signal presence function, the $\overline{\text{SP}}$ pin, indicates whether an active signal is present at the output of the GS6081.

The GS6081 can be powered from either a +3.3V or a +2.5V supply. Power consumption is typically 135mW using a +2.5V power supply with one output enabled.

The GS6081 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.




**GS6081 Functional Block Diagram**

## Revision History

| Version | ECO | PCN | Date | Changes and/or Modifications |
|---|---|---|---|---|
| 4 | 020838 | — | July 2014 | Updated max power and current values in Table 2-2. |
| 3 | 016276 | — | November 2013 | Corrected pin order in Table 1-1 to match proper pin numbering arrangement |
| 2 | 013845 | — | July 2013 | Updated from Draft Data Sheet to Final Data Sheet. |
| 1 | 012266 | — | June 2013 | Updated Table 2-3: AC Electrical Characteristics. Changed the product name to GS6081 (and the DOC ID to PDS-060046) to reflect the production-ready status of the device. |
| 0 | 010383 | — | December 2012 | New document. |

# Contents

# 1. Pin Out

## 1.1 Pin Assignment

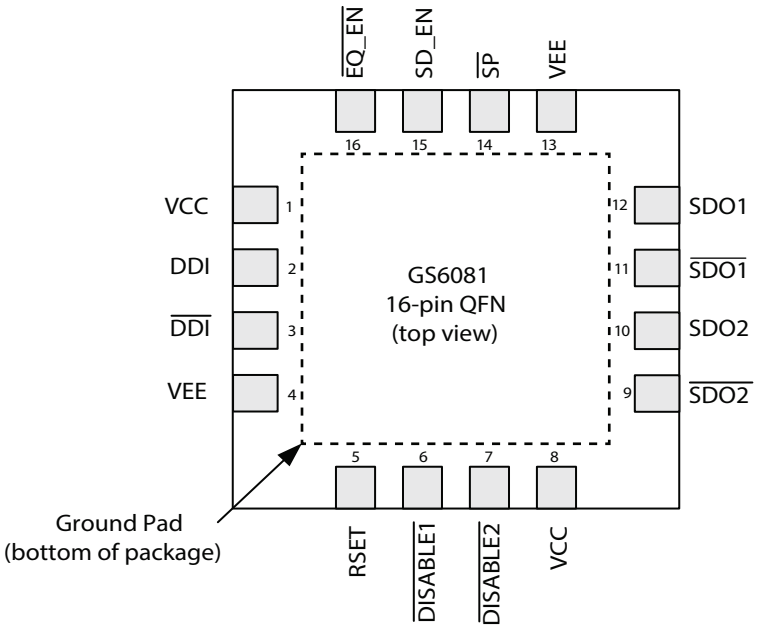



**Figure 1-1: 16-Pin QFN**

## 1.2 Pin Descriptions

### Table 1-1: Pin Descriptions

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1, 8 | VCC | Power | Most positive power supply connection for the input buffer and core.<br>Connect to +3.3V or +2.5V. |
| 2, 3 | DDI, $\overline{\text{DDI}}$ | Input | Serial data differential input.<br>See Section 4.1 for details. |
| 4, 13 | VEE | Power | Most negative power supply connection for the input buffer and core.<br>Connect to ground. |
| 5 | RSET | Input | External output amplitude control resistor connection.<br>See Section 4.6 for details. |

## Table 1-1: Pin Descriptions (Continued)

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 6* | $\overline{\text{DISABLE1}}$ | Input | Output Disable 1 (control signal input).<br>When set LOW, the first serial data output is disabled (powered-down) and the SDO1/$\overline{\text{SDO1}}$ pins are set to high-impedance. When set HIGH, the SDO1/$\overline{\text{SDO1}}$ pins will output a serial data signal.<br>See Section 4.4 for details.<br>This pin has an internal pull-up. |
| 7* | $\overline{\text{DISABLE2}}$ | Input | Output Disable 2 (control signal input).<br>When set LOW, the second serial data output is disabled (powered-down) and the SDO2/$\overline{\text{SDO2}}$ pins are set to high-impedance.<br>When set HIGH, the SDO2/$\overline{\text{SDO2}}$ pins will output a serial data signal.<br>See Section 4.4 for details.<br>This pin has an internal pull-down. |
| 9,10 | $\overline{\text{SDO2}}$, SDO2 | Output | Serial data differential output of second output buffer. |
| 11,12 | $\overline{\text{SDO1}}$, SDO1 | Output | Serial data differential output of first output buffer. |
| 14 | $\overline{\text{SP}}$ | Output | Signal Presence (status signal output).<br>Indicates presence of a signal at the pre-driver to the device's output stage.<br>See Section 4.5 for details. |
| 15 | SD_EN | Input | SD Slew Rate Enable (control signal input).<br>Sets the slew rate for SDO/$\overline{\text{SDO}}$.<br>See Section 4.3.1 for details.<br>This pin has an internal pull-up. |
| 16 | $\overline{\text{EQ\_EN}}$ | Input | Equalizer Enable (control signal input).<br>See Section 4.2 for details.<br>This pin has an internal pull-up.<br>**Note:** this pin must be pulled HIGH or left floating for operation in SD mode. |
| — | Center Pad | Power | Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 16. |

*__Note:__ When pins 6 and 7 are driven LOW together (or similarly when pin 6 is driven LOW while pin 7 is left floating), the entire device is powered-down. In this state, minimum power consumption occurs.

# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

### Table 2-1: Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Supply Voltage | -0.5V to +3.6 $V_{DC}$ |
| Input ESD Voltage | 2.5kV |
| Storage Temperature Range ($T_s$) | -50°C to +125°C |
| Input Voltage Range (any input) | -0.3 to ($V_{CC}$ +0.3)V |
| Operating Temperature Range | -40°C to +85°C |
| Solder Reflow Temperature | 260°C |

**Note:** Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation outside of the ranges shown in Table 2-1 is not implied.

## 2.2 DC Electrical Characteristics

### Table 2-2: DC Electrical Characteristics

$V_{CC}$ = +3.3V ±5% or +2.5V ±5%; $T_A$ = -40°C to +85°C, unless otherwise shown

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.3V Typical | 3.135 | 3.3 | 3.465 | V | — |
| | | 2.5V Typical | 2.375 | 2.5 | 2.625 | V | — |
| Power Consumption (+2.5V) | $P_D$ | SDO1/$\overline{SDO1}$ or SDO2/$\overline{SDO2}$ enabled | — | 135 | 160 | mW | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ enabled | — | 205 | 242 | mW | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ disabled (Power-Down Mode) | — | 3 | 5 | mW | 1 |
| Power Consumption (+3.3V) | $P_D$ | SDO1/$\overline{SDO1}$ enabled, SDO2/$\overline{SDO2}$ disabled | — | 185 | 222 | mW | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ enabled | — | 284 | 340 | mW | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ disabled (Power-Down Mode) | — | 4 | 6 | mW | 1 |

### Table 2-2: DC Electrical Characteristics (Continued)

$V_{CC}$ = +3.3V ±5% or +2.5V ±5%; $T_A$ = -40°C to +85°C, unless otherwise shown

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Current (+2.5V) | $I_S$ | SDO1/$\overline{SDO1}$ or SDO2/$\overline{SDO2}$ enabled | — | 54 | 61 | mA | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ enabled | — | 82 | 92 | mA | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ disabled (Power-Down Mode) | — | 1 | 1.8 | mA | 1 |
| Supply Current (+3.3V) | $I_S$ | SDO1/$\overline{SDO1}$ or SDO2/$\overline{SDO2}$ enabled | — | 56 | 64 | mA | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ enabled | — | 86 | 98 | mA | 1 |
| | | SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ disabled (Power-Down Mode) | — | 1 | 1.8 | mA | 1 |
| Output Voltage | $V_{CMOUT}$ | Common mode | — | $V_{CC}$ - $V_{OUT}$ | — | V | — |
| Input Voltage | $V_{CMIN}$ | Common mode | 1.4 + $\Delta V_{DDI}/2$ | — | $V_{CC}$ - $\Delta V_{DDI}/2$ | V | — |
| SD_EN, $\overline{DISABLE}$, $\overline{EQ\_EN}$ Input | $V_{IH}$ | $I_{IH}$ <= 150µA | 1.7 | — | — | V | — |
| | $V_{IL}$ | $I_{IL}$ <= 150µA | — | — | 0.4 | V | — |
| $\overline{SP}$ Drive Strength | — | — | 2 | — | — | mA | — |

**Notes:**

1. Power consumed in GS6081 only. Termination resistors draw extra current.

# 2.3 AC Electrical Characteristics

### Table 2-3: AC Electrical Characteristics

$V_{CC}$ = +3.3V ±5% or +2.5V ±5%; $T_A$ = -40°C to +85°C, unless otherwise shown

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Serial input data rate | $DR_{SDO}$ | — | 270 | — | 5940 | Mb/s | 1 |
| Additive jitter | — | 5.94Gb/s | — | 15 | — | $ps_{pp}$ | 2, 8 |
| | — | 2.97Gb/s | — | 10 | — | $ps_{pp}$ | 2 |
| | — | 1.485Gb/s | — | 10 | — | $ps_{pp}$ | 2 |
| | — | 270Mb/s | — | 30 | — | $ps_{pp}$ | 2 |

## Table 2-3: AC Electrical Characteristics (Continued)

$V_{CC}$ = +3.3V ±5% or +2.5V ±5%; $T_A$ = -40°C to +85°C, unless otherwise shown

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Rise/Fall time | $t_r$, $t_f$ | 5.94Gb/s | — | 66 | — | ps | 3, 8 |
| | $t_r$, $t_f$ | SD_EN=0 | — | — | 135 | ps | 3 |
| | $t_r$, $t_f$ | SD_EN=1 | 400 | — | 800 | ps | 3 |
| Mismatch in rise/fall time | $\triangle t_r$, $\triangle t_f$ | HD/3G/UHD modes | — | — | 35 | ps | 8 |
| Duty cycle distortion | — | SD_EN=0, 5.94Gb/s | — | 18 | — | ps | 4, 5, 8 |
| | — | SD_EN=0, 2.97Gb/s | — | — | 14 | ps | 4, 5 |
| | — | SD_EN=0, 1.485Gb/s | — | — | 20 | ps | 4, 5 |
| | — | SD_EN=1 | — | — | 50 | ps | 4, 5 |
| Overshoot | — | SD_EN=0, | — | — | 10 | % | 4 |
| Output Return Loss | ORL | 5 MHz – 1.485GHz | 16 | 19 | — | dB | 6 |
| | | 1.485GHz – 2.97GHz | 12 | 15 | — | dB | 6 |
| Output Voltage Swing | $V_{OUT}$ | $R_{SET}$ = 750Ω | 750 | 800 | 850 | $mV_{pp}$ | 4 |
| Input Voltage Swing | $\triangle V_{DDI}$ | Guaranteed functional. | 100 | — | 2200 | $mV_{ppd}$ | — |
| | | Guaranteed to meet all published specifications. | 250 | | 2200 | $mV_{ppd}$ | — |
| Output Disable Delay | — | Any output enabled to all outputs disabled | — | — | 80 | ns | — |
| Output Enable Delay | — | All outputs disabled to any output enabled. | — | — | 4 | µs | — |
| | — | One output enabled to both outputs enabled. | — | — | 500 | ns | 7 |

**Notes:**

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Turning on input trace equalization will reduce jitter in most applications.
3. Rise/Fall time measured between 20% and 80% applies to 800$mV_{pp}$ output swing only.
4. Single-ended into a 75Ω external load.
5. Calculated as the actual positive bit-width compared to the expected positive bit-width using a 1010 pattern.
6. ORL depends on board design. The GS6081 achieves this specification on Semtech's evaluation boards.
7. This Output Enable Delay applies only to the newly enabled output. The output that is already enabled is not impacted in this case.
8. Results based on Validation Data using recommended Application Circuit.

# 3. Input/Output Circuits

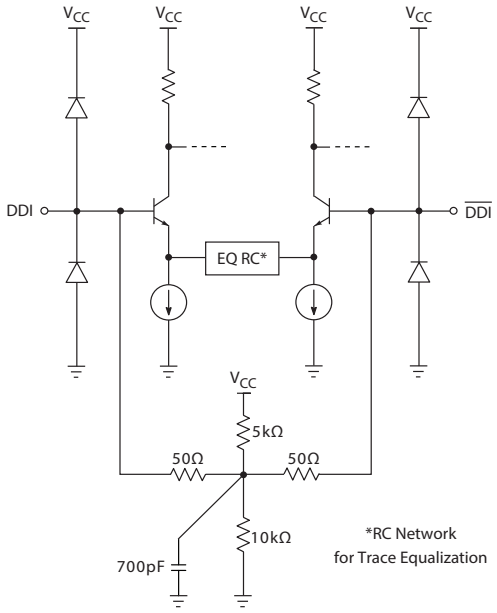



**Figure 3-1: Differential Input Stage (DDI/$\overline{\text{DDI}}$)**

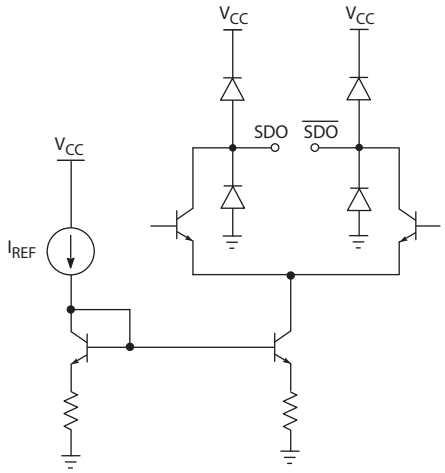



**Figure 3-2: Differential Output Stage (SDO1/$\overline{\text{SDO1}}$, SDO2/$\overline{\text{SDO2}}$)**

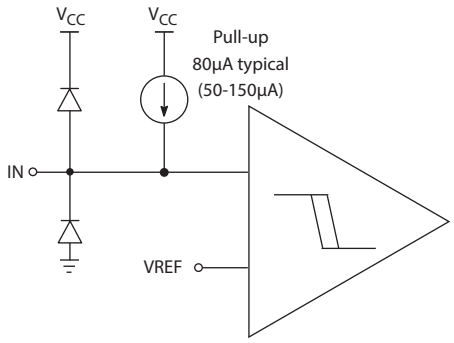



**Figure 3-3: Control Input ($\overline{\text{DISABLE1}}$, SD_EN, $\overline{\text{EQ_EN}}$)**

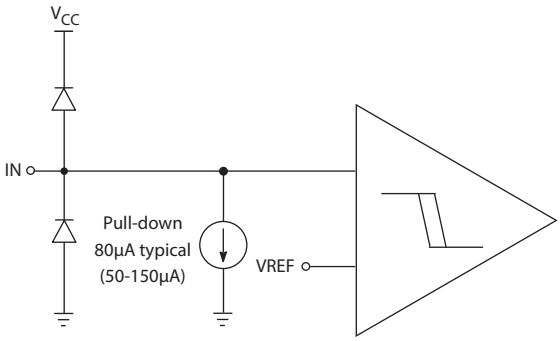



**Figure 3-4: Control Input ($\overline{\text{DISABLE2}}$)**

# 4. Detailed Description

## 4.1 Serial Data Input

The GS6081 features a differential input buffer with on-chip 100Ω differential termination.

The serial data input signal is connected to the DDI and $\overline{\text{DDI}}$ input pins of the device.

Input signals can be single-ended or differential, DC or AC-coupled.

The serial data input buffer is capable of operation with any binary coded signal that meets the input signal level requirements, in the range of 270Mb/s to 5.94Gb/s.

The input circuit is self-biasing to allow for simple AC or DC-coupling of input signals to the device.

## 4.2 Input Trace-equalization

The GS6081 features fixed trace-equalization to compensate for PCB trace dielectric losses.

**Note:** This feature is not available in SD mode, and therefore trace-equalization must be disabled when operating in this mode.

The trace-equalization has two settings, OFF and ON. ON invokes a typical 3dB gain value at 1.5GHz.

**Table 4-1: Input Trace-Equalization**

| $\overline{\text{EQ\_EN}}$ | Function |
|---|---|
| 0 | Typical 3dB Trace Equalization |
| 1 | Trace Equalization OFF |
| Floating | Trace Equalization OFF |

## 4.3 Serial Data Output

The GS6081 features dual current-mode differential output drivers capable of driving up to 1040mV$_{pp}$ single-ended into a 1m length of 75Ω cable terminated at both ends.

The output signal amplitude or is set using an external $R_{SET}$ resistor.

The SDO1/$\overline{\text{SDO1}}$ and SDO2/$\overline{\text{SDO2}}$ pins of the device provide the serial data outputs.

### 4.3.1 Slew Rate Selection (Rise/Fall Time Requirement)

The GS6081 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the SD_EN input pin.

**Table 4-2: Slew Rate Selection**

| SD_EN | Rise/Fall Time |
|---|---|
| 0 | UHD-SDI (5.94Gb/s), SMPTE ST 424 and SMPTE ST 292 compliant |
| 1 | SMPTE ST 259 compliant |
| Floating | SMPTE ST 259 compliant |

## 4.4 Output Disable

The GS6081 supports an output disable function for each serial data differential output.

Control of this function is determined by the setting of the serial output disable ($\overline{\text{DISABLE1}}$ and $\overline{\text{DISABLE2}}$) control pins.

Setting this pin LOW, disable power to the current mode serial data output drivers.

**Table 4-3: Output Disable**

| $\overline{\text{DISABLE1}}$ | $\overline{\text{DISABLE2}}$ | SDO1/$\overline{\text{SDO1}}$ | SDO2/$\overline{\text{SDO2}}$ |
|---|---|---|---|
| 0 | 0 or Floating | All Chip Power Down | |
| 0 | 1 | High-Impedance | Operational |
| 1 or Floating | 0 or Floating | Operational | High-Impedance |
| 1 or Floating | 1 | Operational | Operational |

When $\overline{\text{DISABLE1}}$ and $\overline{\text{DISABLE2}}$ are driven LOW simultaneously, the entire device is powered down, and the power consumption is minimized.

## 4.5 Signal Presence Indicator ($\overline{\text{SP}}$)

The GS6081 supports a signal presence indicator function.

The signal presence pin ($\overline{\text{SP}}$) is an active-low output that indicates a signal has been detected at the pre-driver output.

The signal presence function measures signal-edge energy to indicate that the pre-driver to the serial data outputs is toggling.

**Table 4-4: Signal Presence Indicator**

| Pre-Driver Output | $\overline{SP}$ Pin |
|---|---|
| Signal present | 0 |
| No signal present | 1 |

# 4.6 Output Amplitude (RSET)

The output amplitude of the GS6081 can be adjusted by changing the value of the $R_{SET}$ resistor as shown in Figure 4-1. For an 800m$V_{pp}$ output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The $R_{SET}$ resistor is part of an internal DC feedback loop in the GS6081. The resistor should be placed as close as possible to the RSET pin, and connected directly to the $V_{CC}$ plane (traces/wires may cause instability).

**Note:** Care should be taken when considering layout of the $R_{SET}$ resistor. Please refer to Section 5.1 for more details.

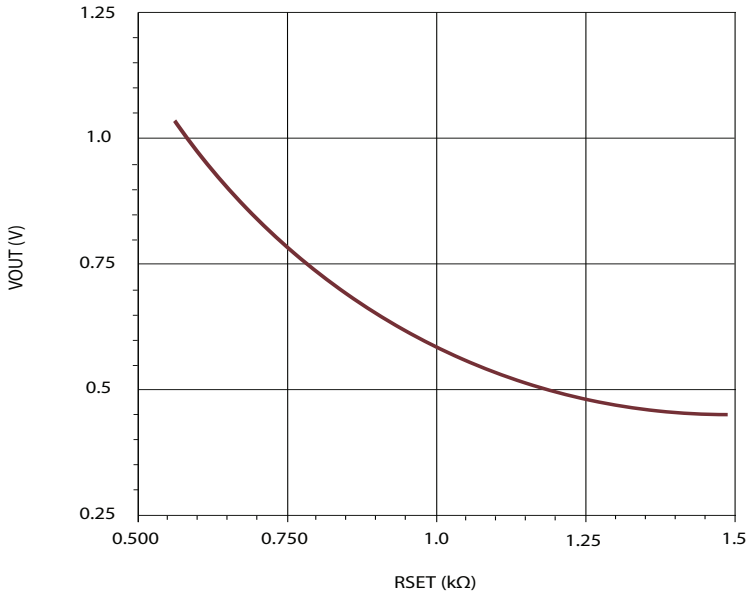



**Figure 4-1: $V_{OUT}$ vs. $R_{SET}$**

In order to determine the best starting value for $R_{SET}$, the following formula should be used:

**Rset = 8*(Rtrm/VoutppSE)**

Where **VoutppSE** is in Volts, and both resistances are in Ω.

**Rtrm** is the value of the termination resistors, which should be equal to the characteristic impedance of the cable, and is typically 75Ω.

The cable must be short (≤1m), and terminated at both ends for the formula to be valid.

Example: For a 75Ω cable, Rtrm = 75Ω (at both ends), VoutppSE = 800m$V_{pp}$

**Rset = 8*(75/0.8) = 750Ω**

This formula is not valid for long, unterminated, or improperly terminated cables.

This formula should be considered as a starting point, and actual swing values may vary based on layout.

### Table 4-5: Typical $R_{SET}$ Values

| Output Swing ($mV_{pp}$) | $R_{SET}$ (Ω) |
|---|---|
| 1040 | 576 |
| 800 | 750 |
| 500 | 1210 |

# 4.7 Output Return Loss Measurement

The GS6081 has a feature designed to facilitate reliable output return loss (ORL) measurement while the device is still powered. The device can be put into a BALANCE mode which prevents the outputs from toggling while the device is powered on, allowing the ORL to be measured while the device is still powered.

When $\overline{\text{EQ\_EN}}$ is LOW while SD_EN is HIGH, the device goes into BALANCE mode. This mode is used during ORL measurement, disabling the AC signal path of the device without powering it down. When in BALANCE mode, the device produces equal pull-down currents in both differential shoulders of both serial data differential outputs, effectively stopping all outputs at the output common mode voltage level. Semtech recommends using BALANCE mode when measuring ORL with +2.5V termination voltage.

# 5. Application Information

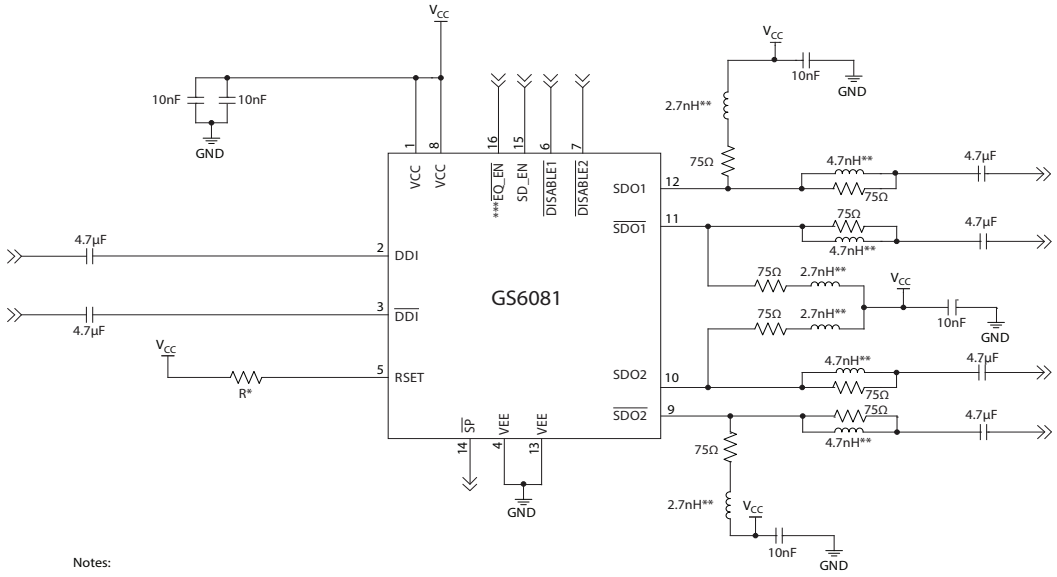
## 5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance
- The PCB ground plane is removed under the GS6081 output components to minimize parasitic capacitance (**Note:** care should be taken, as removing too much of the plane will make the system susceptible to EMI)
- The PCB ground plane is removed under the GS6081 RSET pin and resistor to minimize parasitic capacitance. The $R_{SET}$ resistor should be directly connected to the VCC plane
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high-speed traces
- High-speed traces are round-curved (rather than 45° or 90° angles) to minimize impedance variations due to change of PCB trace width

## 5.2 Typical Application Circuit




Notes:

* Selection based on desired output swing and PCB layout.

** Typical value: varies with layout, and represents a trade-off between good eye shape and output return loss.

For backward compatibility with previous generation Cable Drivers;
2.7nH -> 0W
4.7nH -> 5.6nH

*** Please refer to section 4.2.

**Figure 5-1: Typical Application Circuit**

# 6. Package & Ordering Information

## 6.1 Package Dimensions

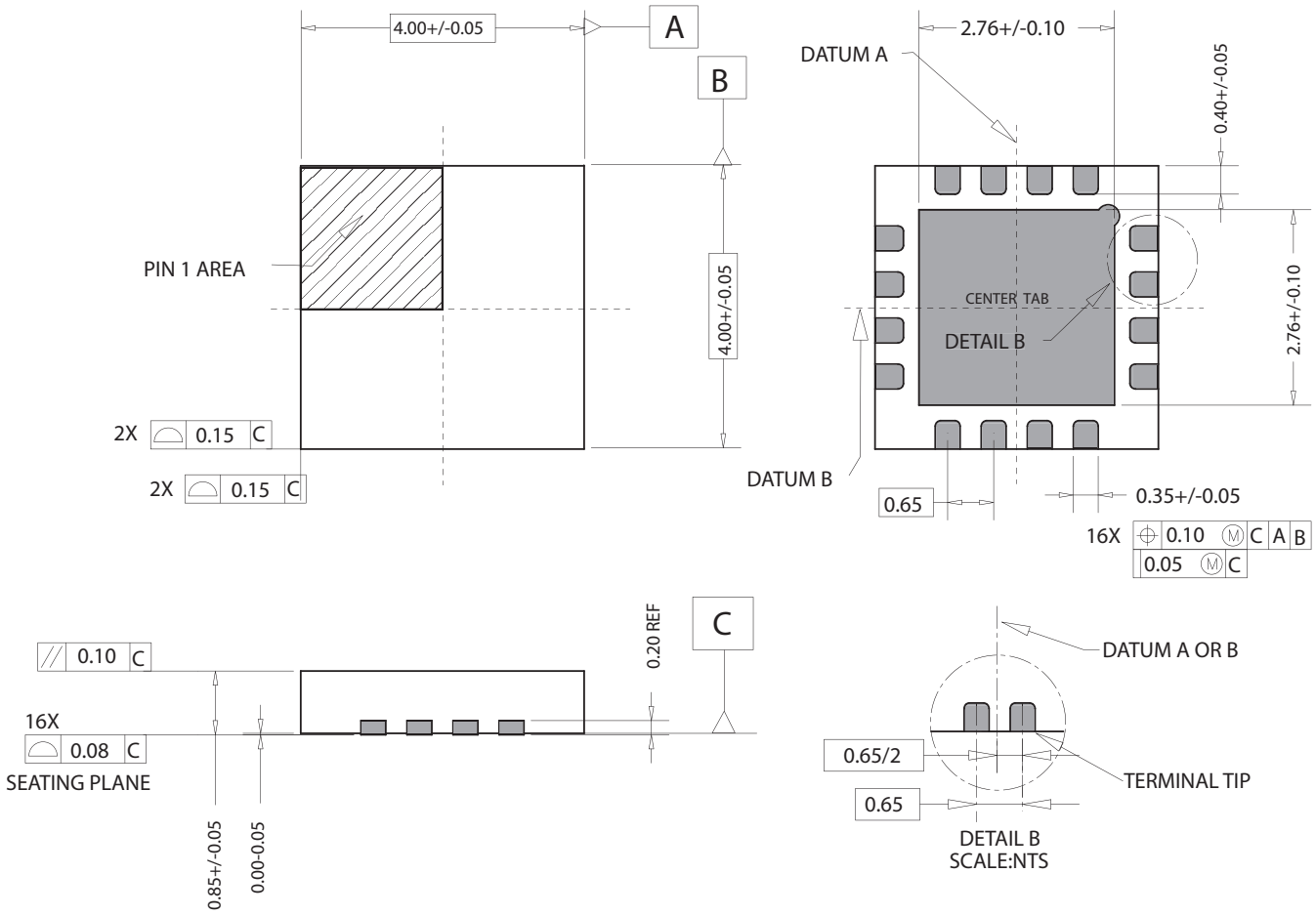



**Figure 6-1: Package Dimensions**

# 6.2 Recommended PCB Footprint

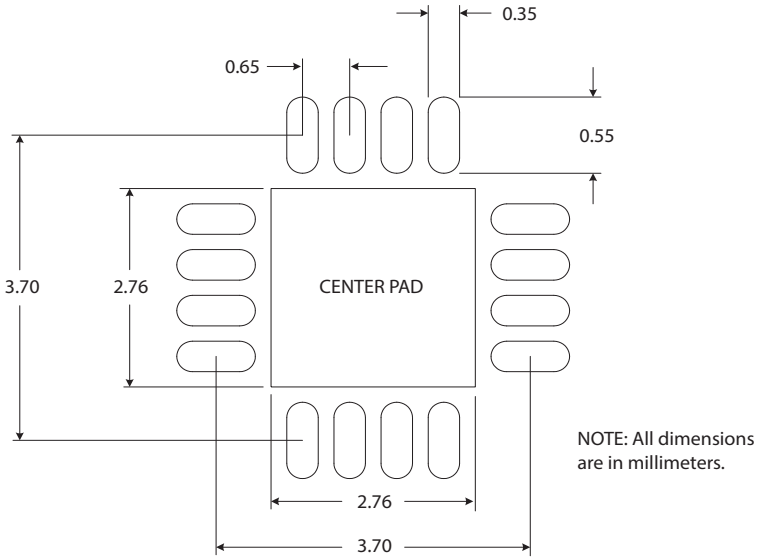



**Figure 6-2: Recommended PCB Footprint**

The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

**Note:** Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

# 6.3 Packaging Data

### Table 6-1: Packaging Data

| Parameter | Value |
|---|---|
| Package type / dimensions / pad pitch | 16-pin QFN / 4mm x 4mm / 0.65mm |
| Package Drawing Reference | JEDEC M0220 |
| Moisture Sensitivity Level | 1 |
| Junction to Case Thermal Resistance, $\theta_{j-c}$ | 31.0°C/W |
| Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow) | 43.8°C/W |
| Psi, $\Psi$ | 11.0°C/W |
| Pb-free and RoHS compliant, Halogen-free | Yes |

# 6.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-3.

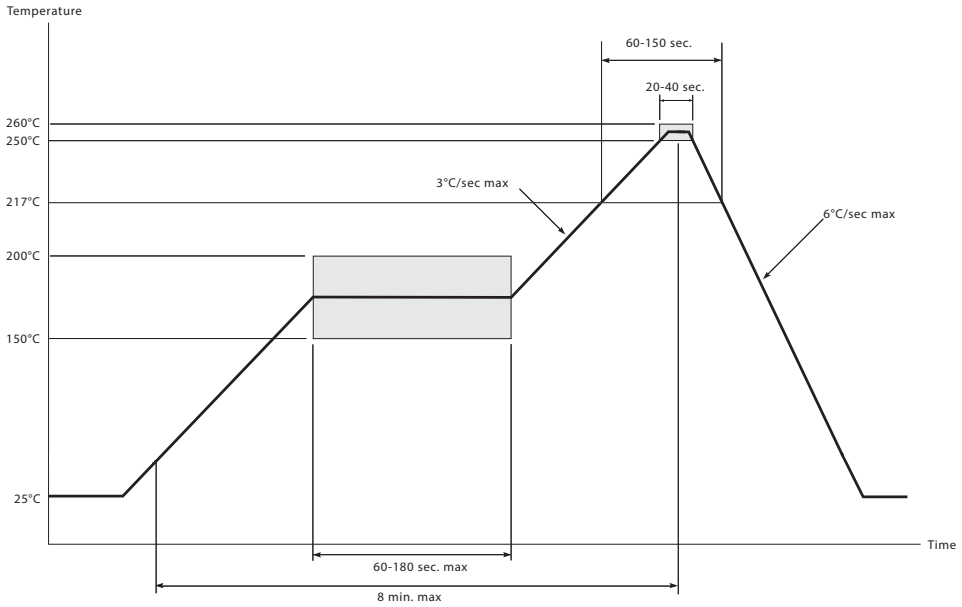
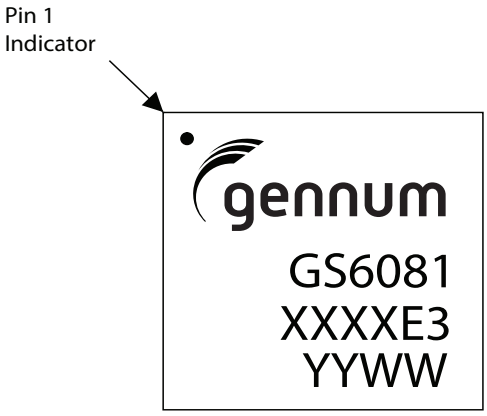



**Figure 6-3: Maximum Pb-free Solder Reflow Profile**

# 6.5 Marking Diagram




XXXX - Last 4 digits (excluding decimal) of SAP Batch Assembly (FIN) as listed on Packing Slip.
E3 - Pb-free & Green indicator
YYWW - Date Code

**Figure 6-4: Marking Diagram**

# 6.6 Ordering Information

### Table 6-2: Ordering Information

| | Part Number | Package | Temperature Range |
|---|---|---|---|
| GS6081 | GS6081-INE3 | 16-pin QFN | -40°C to 85°C |
| GS6081 | GS6081-INTE3 | 16-pin QFN<br>250pc Reel | -40°C to 85°C |

**DOCUMENT IDENTIFICATION**
**FINAL DATA SHEET**

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**CAUTION**

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION



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